DINI GROUP

LOGIC Emulation Source

User Manual DN-DualV6-PCIe-4

LOGIC EMULATION SOURCE

DN-DualV6-PCIe-4 User Manual Version 2.0

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© Dini Group
7469 Draper Ave.
La Jolla, CA92037
Phone 858.454.3419 • Fax 858.454.1728
support@dinigroup.com
www.dinigroup.com

Table of Contents

List of Figures

List of Tables

Chapter

1

Introduction

This User Manual accompanies the DN-DualV6-PCIe-4 Xilinx Virtes-6 Logic Emulation Board. For specific information regarding the Virtex-6 parts, please reference the datasheet on the Xilinx website.

1 DN-DualV6-PCIe-4 LOGIC Emulation Kit

The DN-DualV6-PCIe-4 is hosted in a 4-lane PCI Express (GEN1) system but can be used stand-alone and is configured via USB or Ethernet. The FPGA configuration and other miscellaneous board functions are controlled by the Marvell MV78200 CPU. A single DN-DualV6-PCIe-4 configured with two Xilinx Virtex-6 (SX475T) FPGAs can emulate up to 10 million gates of logic as measured by a reasonable ASIC gate counting standard. This gate count estimate number does not include embedded memories and multipliers resident in each FPGA.

The DN-DualV6-PCIe-4 provides dual Xilinx Virtex-6 FPGAs in the 1156-pin package. The architecture of the board, maximizes interconnect by providing a number of dedicated busses between the FPGAs. The Marvell MV78200 CPU in conjunction with the Configuration FPGA (Virtex-5) is used to configure the Virtex-6 FPGAs using the SelectMAP configuration mode. The Marvell MV78200 provides a number of high-speed interfaces that is available to the user after configuration. The PCI Express interface between the Marvell MV78200 and the Configuration FPGA provides a high-speed data path to the system interface, whether that is USB, Ethernet or PCI Express. A Linux kernel provides the basic services and device drivers used by all other programs running on the Marvell CPU.

Numerous clocking options exist to allow for a flexible clocking scheme. External memory to the Virtex-6 FPGAs is realized using a 64 bit, 204 pin SODIMM that accepts PC3-8500 DDR3 SODIMMs. One 400 pin MEG-Array connector on the bottom of the printed circuit board assembly (PCBA) is used to interface to other Dini Group products, e.g. DNMEG_Obs Daughter Card.

2 DN-DualV6-PCIe-4 Logic Emulation Board Features



Figure 1 - DN-DualV6-PCIe-4 Logic Emulation Board

DN-DualV6-PCIe-4 Virtex-6 Board features the following:

- Hosted in a 4-lane PCI Express Slot (GEN1) or Stand-alone
- Xilinx Virtex-6 FPGAs (FF1156), -3, -2, -1, -1L Speed Grade, populated with any of the following options for FPGA A/B:
    - XC6VSX475T
    - XC6VSX315T
    - XC6VLX365T
    - XC6VLX240T
    - XC6VLX195T
    - XC6VLX130T
- FPGA to FPGA interconnect, Single-ended and LVDS
    - 500MHz LVDS Chip-to-Chip (1.0Gb/s)
    - Source Synchronous Clocking for LVDS
    - LVDS pairs can be used as two single-ended signals at reduced frequency (~225MHz)
    - Reference designs for integrated I/O pad ISERDES/OSERDES
    - 10x pin multiplexing per LVDS pair
- Not Main Bus(NMB) connects both Virtex-6 FPGAs via dedicated busses to the Configuration FPGA

    - 40 Signals, LVDS
- RocketIO GTX Transceivers
    - 6.5 Gb/s (with -3, -2 speed grade)
    - 5.0 Gb/s with -1
    - 4-Lanes connected between FPGA A and FPGA B
    - Lanes connected from Configuration FPGA to FPGA A
    - Lanes connected from Configuration FPGA to FPGA B
    - Data examples provided using Aurora protocol
- FPGA Configuration (Virtex-6)
    - Configuration Options - USB, PCIe, Ethernet, JTAG
    - Stand-alone configuration with USB stick
    - Encryption, Readback and Partial Reconfiguration
- Flexible Clock Resources
    - FPGA Clock Multipliers - Si5326 (x3)
        - General Clock Network (G0)
        - DDR3 Clock Network (G1)
        - LVDS Clock Network (G2)
    - External FPGA Clock (LVDS) Input via Test Point
    - Multiple clocks from the Daughter Card Header
    - Multiplexed Global clocks from FPGA A/B
    - Clock Test Points (x3)
    - Oscillators for GTP Transceivers (x4)
- CPU - Marvel MV78200 Discovery Innovation (Dual)
    - CPU Clocks – up to 1 GHz
    - Dual USB2.0 ports (Type B connector)
    - Dual Serial-ATA II (SATA)
    - Gigabit Ethernet interface, 10/100/1000 GbE (RJ45)
    - DDR2, 4GB (128M x 64)
    - Sheeva™ CPU Core (ARMv5TE compliant)
        - Out-of-order execution
        - Single and double-precision IEEE compliant floating point

        - 16-bit Thumb instruction set increases code density
        - DSP instructions boosts performance for signal processing applications
        - MMU to support virtual memory features
        - Dual Cache: 32 KB for data and instruction, parity protected
        - L2 cache: 512 KB unified L2 cache per CPU (total of 1MB), ECC protected.
    - 4 GB external DDR2 SDRAM
        - Organized in a 128M x 64 configuration
        - 400 MHz (800 MHz data rate)
    - After configuration, both CPUs are dedicated entirely to user application
    - LINUX operating system
        - Source and examples provided via GPL license (no charge)
- Memory
    - DDR3, 4GB (128Meg x 64), 204 pin SODIMM (PC3-8500)
    - Serial FLASH Memory, 64Kb (8192 x 8)
- Daughter Card Header (x1) LVDS – MEG-Array (400 pin)
    - 93 LVDS unidirectional pairs + clocks (or 186 single-ended)
    - 650 MHz on all signals with source synchronous LVDS
    - Signal voltage set by daughter card (+1.2V to +2.5V)
    - +12V (24W max) and +3.3V (10W max), Supplied power rails (fused
- User LEDs
- Onboard Distributed Power Supplies
- Full support for Embedded Logic Analyzers
    - ChipScope Logic Analyzer
- Shared RS232 Port, 10 pin Header
- Stand Alone operation, requires an external +12V ATX power supply with a PCIe power connector.

3 Package Contents:

Before using the kit or installing the software, be sure to check the contents of the kit and inspect the board to verify that you received all of the items. If any of these items are missing, contact Dini Group before you proceed. The DN-DualV6-PCIe-4 Logic Emulation Board kit includes the following:

- USB Flash Drive (2GB)
- USB 2.0 Cable
- RS232 DB9(F) to IDC Header Cable, 12"
- RS232 Serial Cable (DB9), 6ft, F/F
- Ethernet Cable (RJ45), 6ft, P/N CC5E-B25B
- 6-Pin PSU Adaptor for PCI Express Video Cards
- PSU Enable Connector
- Daughter Card Mounting Hardware
    - Screw, Machine M3x5mm (x4)
    - Nut, HEX M3 (x4)
    - Spacer, M3x14mm (x4)
- Lithium Coin Battery (CR1220)
- Customer Support Package (USB Flash Drive)
    - Host Software (EMU)
    - Virtex-6 Reference Designs (Verilog)
    - User Manual (pdf format)
    - Schematic (pdf format)
    - Component Datasheets (pdf format)

Optional items that support development efforts (not provided):

✓ Xilinx ISE Software

- ✓ Xilinx Platform Cable USB
- ✓ DDR3 SODIMMs (Available upon request)

4 Inspect the Board

Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment. Verify that all components are on the board and appear intact.

5 Additional Information

For additional information, please visit http://www.dinigroup.com/. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
User Manual	This is the main source of technical information. The manual should contain most of the answers to your questions
Demonstration Videos	MEG-Array Daughter Card header insertion and removal video
Dini Group Web Site	The web page will contain the latest user manual, application notes, FAQ, articles, and any device errata and manual addenda. Please visit and bookmark: http://www.dinigroup.com
Data Book	Pages from Virtex-6 Databook, which contains device-specific information on Xilinx device characteristics
E-Mail	You may direct questions and feedback to Dini Group using this e-mail address: support@dinigroup.com
Phone Support	Call us at **858.454.3419** during the hours of 8:00am to 5:00pm Pacific Time.
FAQ	The download section of the web page may contain a document called **DN-DualV6-PCIe-4 Frequently Asked Questions (FAQ)**. This document is periodically updated with information that may not be in the User's Manual.

Chapter

2

Getting Started

Congratulations on your purchase of the DN-DualV6-PCIe-4 Xilinx Virtes-6 Logic Emulation Board. The remainder of this chapter describes how to start using the DN-DualV6-PCIe-4 Xilinx Virtes-6 Logic Emulation Board.

1 Before You Begin

1.1 Configuring the Programmable Components

The DN-DUALV6-PCIE-4 has been factory tested and pre-programmed to ensure correct operation. The user does not need to alter any jumpers or program anything to see the board work.

1.2 Warnings

- **Daughter Card Test Headers (Over Voltage)** - The 400-pin daughter card test headers are **NOT** 5V tolerant. These signals connect directly with the FPGA IO. Take care when handling the board to avoid touching the components and daughter card connections due to ESD.

- **Mechanical Stress** – Board stiffeners are provided to reduce mechanical stress; however, inserting and removing Daughter Cards may add additional stress that may cause board failures.

- **ESD Warning** - The board is sensitive to static electricity, so treat the PCB accordingly. The target markets for this product are engineers that are familiar with FPGAs and circuit boards. However, if needed, the following web page has an excellent tutorial on the "Fundamentals of ESD" for those of you who are new to ESD sensitive products:

  http://www.esda.org/basics/part1.cfm

- **Operating Temperature** - Avoid touching the PTH012050WAZ power supply modules (PSU6 and PSU10) as they operate at high temperatures and may cause skin burns.

2 Installing the Software

For complete information regarding the Host Software (GUI) and installation instructions, see the "EMU Software Manual" available on the Customer Support Package (USB Flash Drive).

2.1 Exploring the Customer Support Package

The USB Flash Drive contains the following items, see Figure 2:

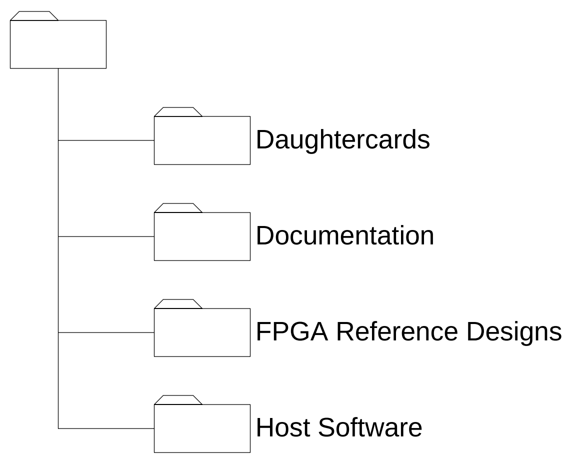


Figure 2 - USB Flash Drive Directory Structure

A description of the USB Flash Drive directory contents is listed in Table 1. Please visit the Dini Group website for the most recent revision of these documents.

Table 1 – USB Flash Drive Directory Contents

USB Flash Drive Directory Contents	
Directory Name	**Description of Contents**
Daughtercards	Complete documentation on the DNMEG_Intercon and the DNMEG_Obs Daughter Cards.
Documentation	Contains the Datasheets, Schematics and User Manual for the board.
FPGA Reference Designs	Contains the source and compiled programming files for the DN-DUALV6-

	PCIE-4 reference designs.
Host Software	Provides the Host Software for the Windows and Linux platforms, including the EMU Software Manual.

3 Board Setup

The instructions in this section explain how to install the DN-DUALV6-PCIE-4 Logic Emulation Board. For the purpose of this demonstration, the DN-DUALV6-PCIE-4 will be configured in Stand-Alone mode.

3.1 Before Powering Up the Board

Before powering up the board, prepare the board as follows:

1. Attach an ATX Power Supply to the "PCIE PWR" header (J5) on the DN-DUALV6-PCIE-4 Logic Emulation Board.

2. Connect the "Ethernet Cable" to the "ETHERNET" header (J3) on the DN-DUALV6-PCIE-4 Logic Emulation Board.

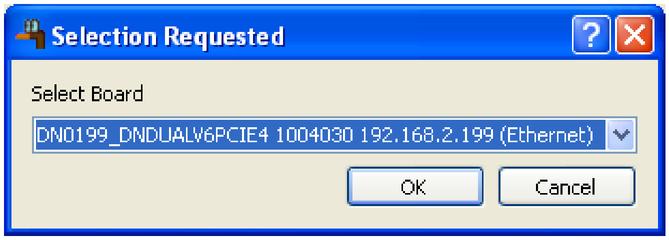
3. If the kit contains Memory SODIMMs, populate the SODIMM sockets. Insert a DDR3 SDRAM SODIMM module into positions J14/J21 – P/N MT8JSF12864HZ-1G4F1. Note: Ensure voltage jumper JP2/JP3 is set to +1.5V, pin 3-1.

4. Install the "EMU" graphical user interfaces software, available on the Customer Support Package (USB Flash Drive). Note: Reference the "EMU Software Manual" regarding driver installation.

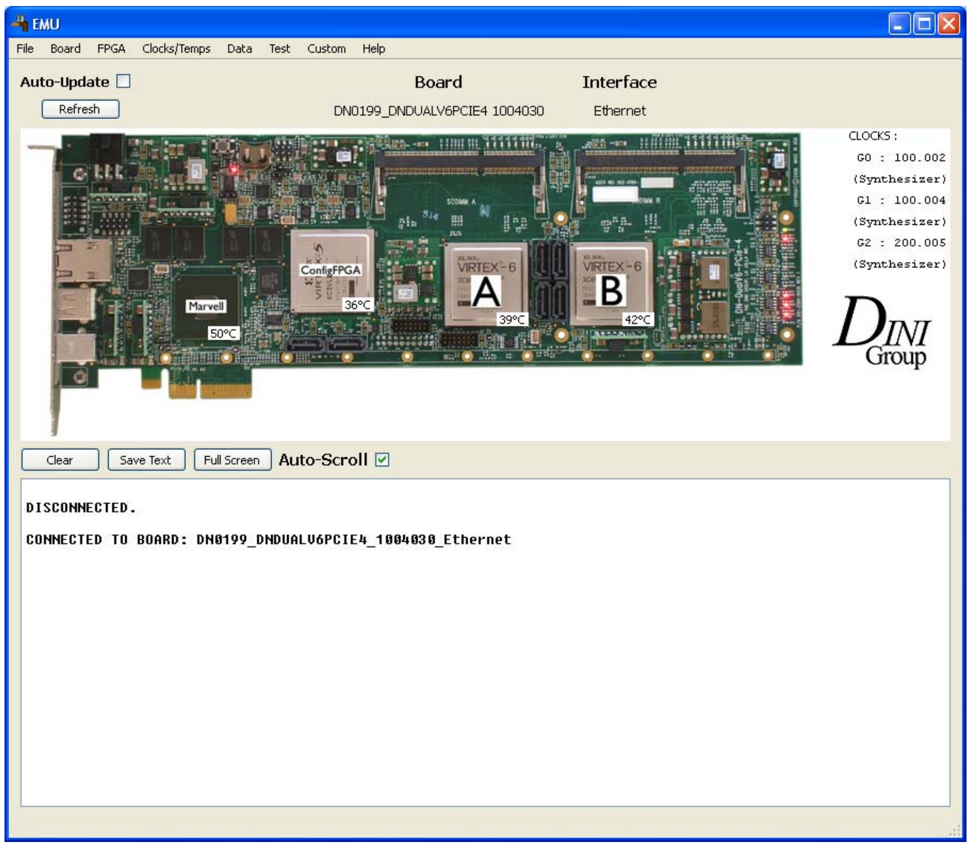
3.2 Powering Up the Board

5. Power up the board by turning ON the ATX power supply and verify the "+12V" LED (DS44) is ON indicating the presence of +12V (located at the right-side of the PCB).

6. Open the "EMU" application and select "Board" followed by "Select Board" (select the "DN0199_DNDUALV6PCIE4 xxxxxxx 192.168.2.199 (Ethernet)" board in the drop-down list that matches the serial number of your board.



7. Verify that the board was correctly identified as a “DN0199_DNDUALV6PCIE4 xxxxxxx” in the window. Note: The serial number will be different.



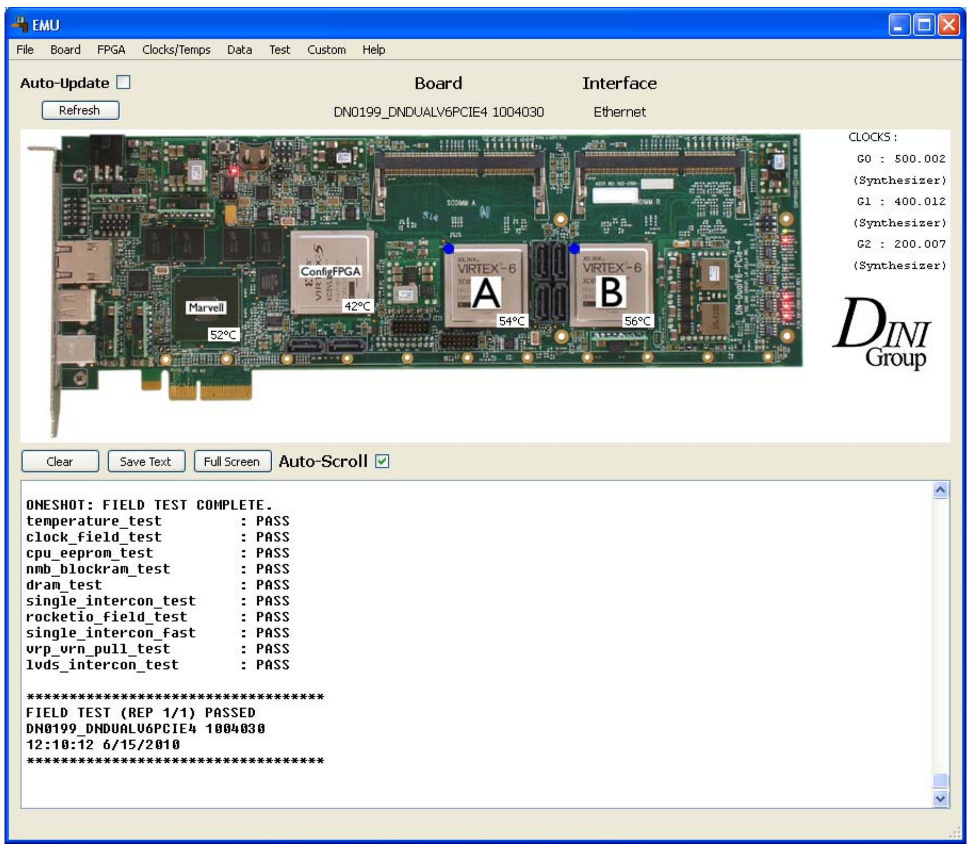
4 Running the Field Test

Select “Test” followed by “Field Test”. The progress of the tests will be displayed in the EMU log window. The following tests will be executed:

- temperature_test
- clock_field_test
- cpu_eeprom_test

- nmb_blockram_test
- dram_test
- single_intercon_test
- rocketio_field_test
- single_intercon_fast
- vrp_vrn_pull_test
- lvds_intercon_test

Verify that the all the Field tests PASSED.



Chapter

3

Programming/Configuring the Hardware

This chapter details the programming and configuration instructions for the DN-DualV6-PCIe-4 Xilinx Virtes-6 Logic Emulation Board.

1 Introduction

This section of the User Manual presents different methods to configure the Xilinx Virtex-6 FPGAs:

- **Configuring the Virtex-6 FPGAs using EMU** – using the Graphical User Interface (GUI).

- **Configuring the Virtex-6 FPGAs using JTAG** – using the Xilinx "Platform Cable USB" and JTAG.

- **Updating the Marvell MV78200 Software** – lists the procedure to update the Marvell MV78200 software.

Virtex-6 FPGAs are configured by loading application-specific configuration data - the bitstream - into internal memory. Because the Xilinx FPGA configuration memory is volatile, it must be configured each time it is powered-up. The bitstream is loaded into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes. The following configuration modes are supported:

- Slave SelectMAP (parallel) configuration mode (x8)
- JTAG/Boundary-Scan configuration mode

The configuration modes are explained in detail in Chapter 2, Configuration Interfaces of the UG360 - Virtex-6 FPGA Configuration User Guide. The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0]. In Slave SelectMAP mode, FPGA A and FPGA B are independently configured from the Configuration FPGA.

2 EMU Graphical User Interface (GUI)

EMU is both an end user application for interacting with Dini Group hardware as well as a development kit for extending EMU's capabilities or writing custom applications. EMU is designed to interface with any Dini Group board that comes with the Marvell processor, see Figure 3. EMU compiles into both a command-line menu-system program (CMD version) and a graphical interface program (GUI version), supporting all functionality in both versions.

EMU supports Windows and Linux platforms, using the QT windowing package for cross-platform support of native GUI interfaces. QT is freely available from the internet and is required for the GUI versions of EMU. It is recommended to use the QT environment in EMU development, but the CMD version can be built without it, using other standard environments such as GCC and MSVC.

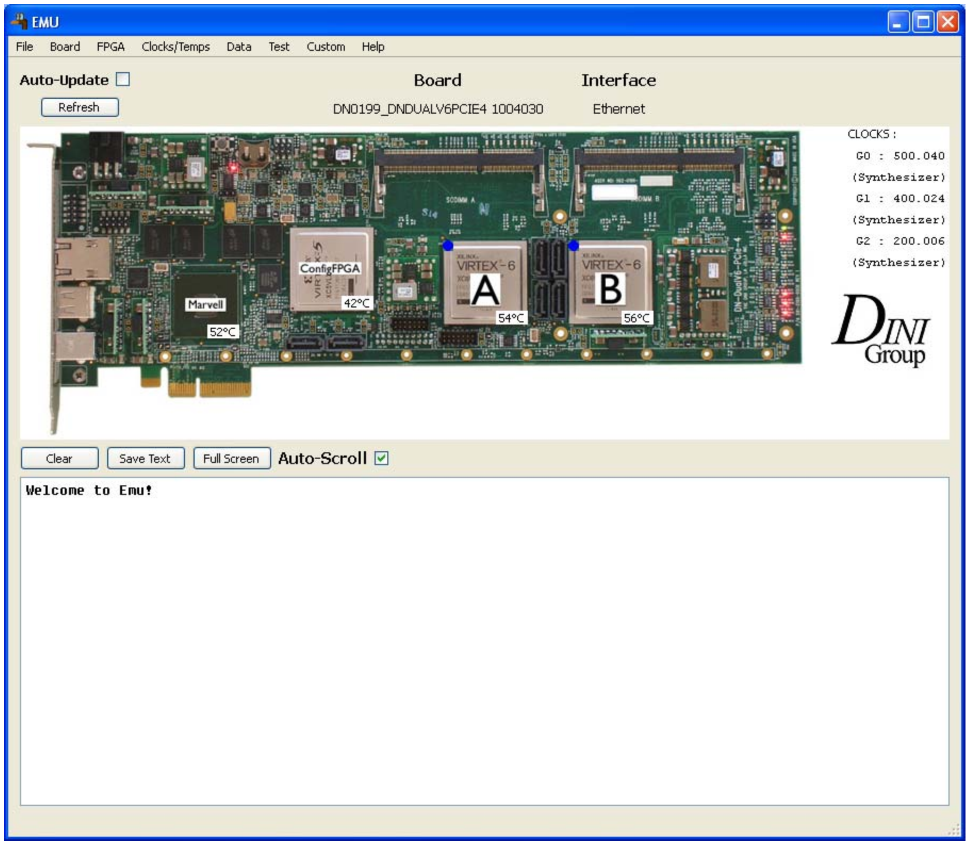


Figure 3 - EMU Graphical User Interface

For more information regarding EMU, please reference the "EMU Software Manual" available on the Customer Support Package (USB Flash Drive).

3 Configuring the Virtex-6 FPGAs using EMU

This section lists detailed instructions for programming the Xilinx Virtex-6 FPGAs using EMU software application. Before configuring the FPGAs, ensure that the EMU software and the driver software are installed on the host computer. The procedure for configuring the FPGAs is the same whether the board is hosted via Ethernet, USB or PCI Express. For the purpose of this example, the Ethernet interface will be demonstrated. . Note: The Configuration FPGA must be configured in order to drive the FPGA A and FPGA B "CSI_B_0" chips select signals.

Note: This User Manual will not be updated for every revision of the EMU software application, so please be aware of minor differences.

3.1 Before Powering Up the Board

Before powering up the board, prepare the board as follows:

1. Attach an ATX Power Supply to the "PCIE PWR" header (J5) on the DN-DUALV6-PCIE-4 Logic Emulation Board.

2. Connect the "Ethernet Cable" to the "ETHERNET" header (J3) on the DN-DUALV6-PCIE-4 Logic Emulation Board. Note: In order to be able to access the board over the network, the network must support DHCP.

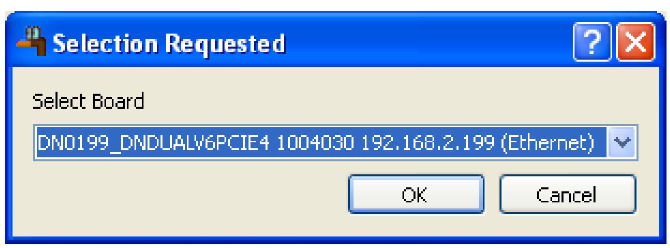
3. If the kit contains Memory SODIMMs, populate the SODIMM sockets. Insert a DDR3 SDRAM SODIMM module into positions J14/J21 – P/N MT8JSF12864HZ-1G4F1. Note: Ensure voltage jumper JP2/JP3 is set to +1.5V, pin 3-1.

4. Install the "EMU" graphical user interfaces software, available on the Customer Support Package (USB Flash Drive). Note: Reference the "EMU Software Manual" regarding driver installation.

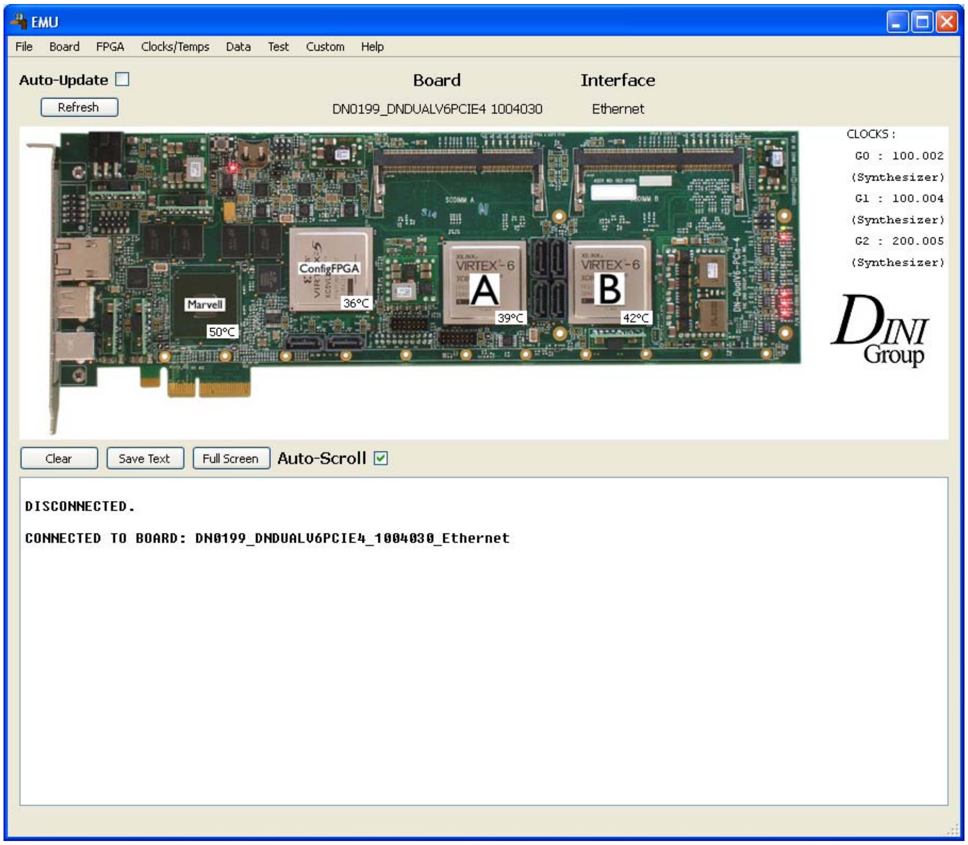
3.2 Powering Up the Board

5. Power up the board by turning ON the ATX power supply and verify the "+12V" LED (DS44) is ON indicating the presence of +12V (located at the right-side of the PCB).

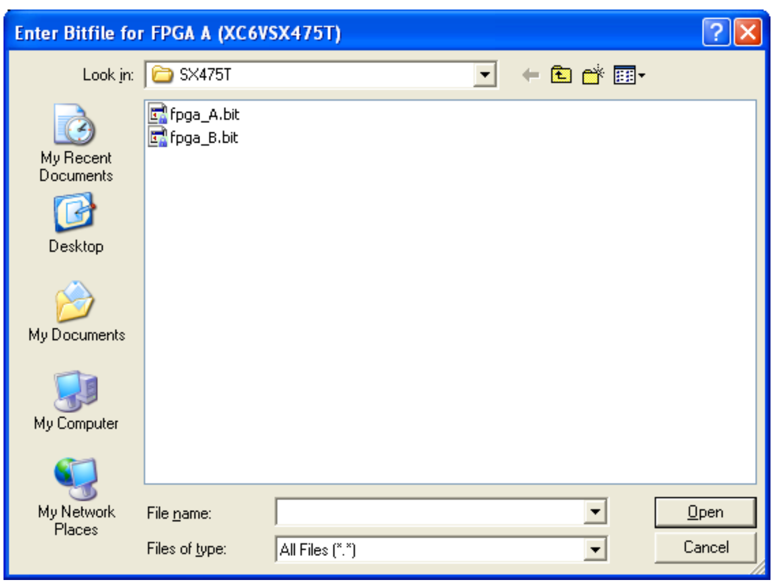
6. Open the "EMU" application and select "Board" followed by "Select Board" (select the "DN0199_DNDUALV6PCIE4 xxxxxxx 192.168.2.199 (Ethernet)" board in the drop-down list that matches the serial number of your board.



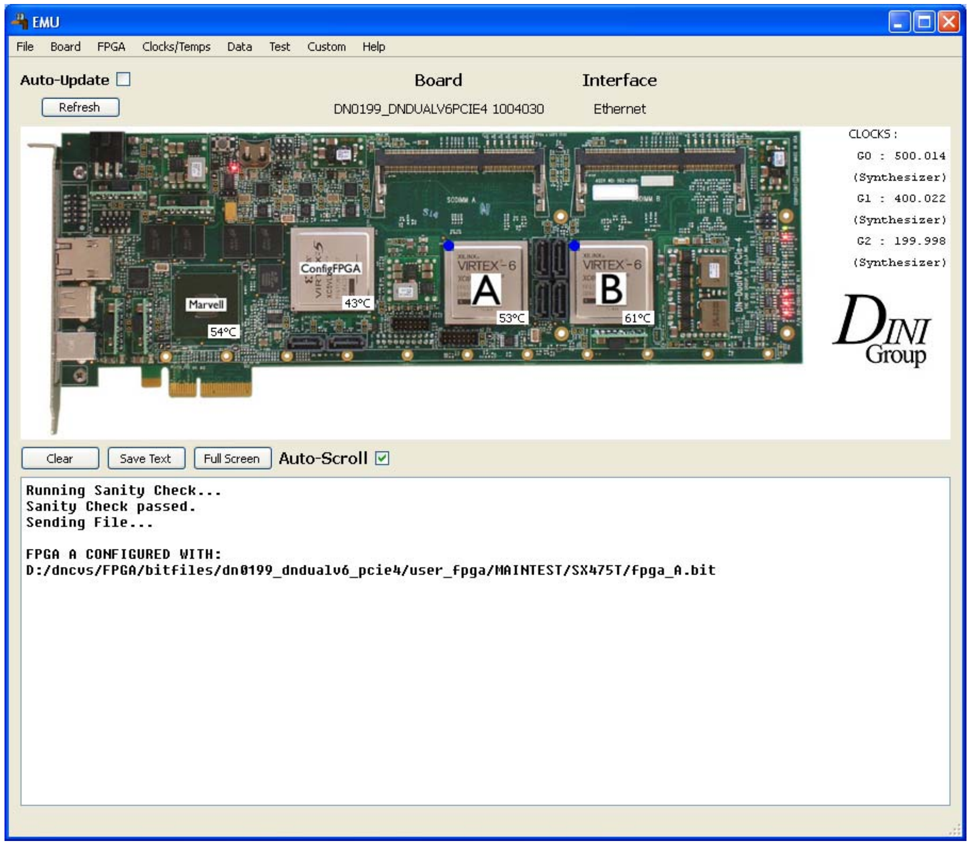
7. Verify that the board was correctly identified as a "DN0199_DNDUALV6PCIE4 xxxxxxx" in the window. Note: The serial number will be different.



8. Right-click on the FPGA to be configured and assign the required bitfile.



9. EMU will perform a sanity check on the bit file and configure the FPGA.



10. Verify that the "FPGAA_DONE" blue LED (DS22 for FPGA A) is enabled, indicating successful configuration of the FPGA.

4 Configuring the Virtex-6 FPGAs using JTAG

This section lists detailed instructions for programming the Xilinx Virtex-6 FPGAs using iMPACT, Version 11.1 tools. Before configuring the FPGA, ensure that the Xilinx software and the "Xilinx Platform Cable USB" driver software are installed on the host computer. The JTAG/Boundary-Scan configuration interface is always available, regardless of the Mode pin settings. The JTAG/Boundary-Scan configuration mode disables all other configuration modes to prevent conflicts between configuration interfaces.

Note: This User Manual will not be updated for every revision of the Xilinx ISE tools, so please be aware of minor differences.

4.1 Setup - Configuring the Virtex-6 FPGAs using JTAG

Before configuring the FPGA, ensure the following steps have been completed:

1. Attach an ATX Power Supply to the "PCIE PWR" header (J5) on the DN-DUALV6-PCIE-4 Logic Emulation Board.

2. Connect the "Xilinx Platform Cable USB" to the "JTAG V6" header (J13).

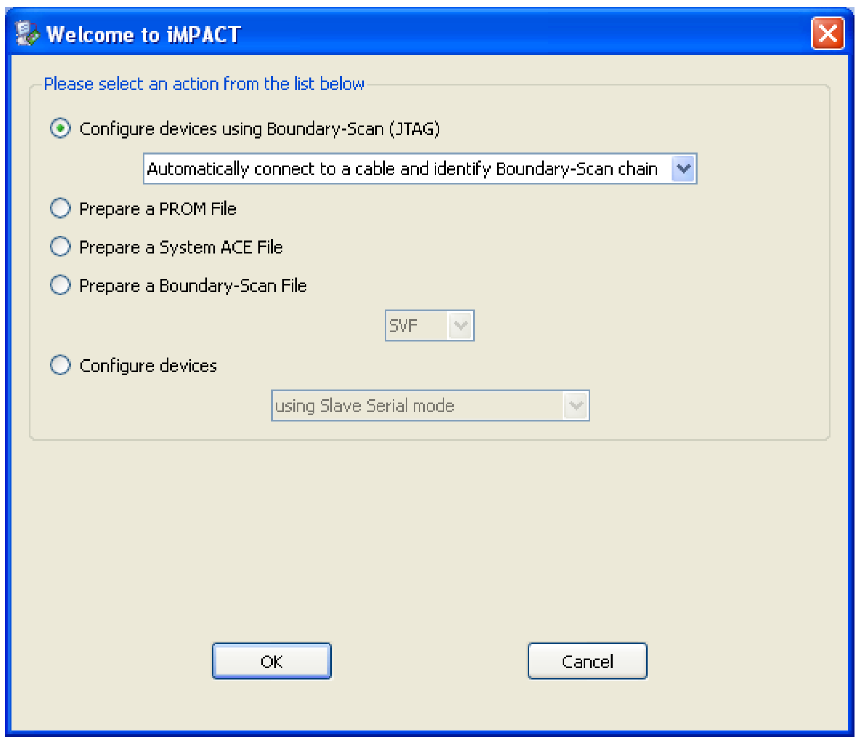
4.2 Powering Up the Board

3. Power up the board by turning ON the ATX power supply and verify the "+12V" LED (DS44) is ON indicating the presence of +12V (located at the right-side of the PCB).

4.3 Configuring the FPGA

To configure the Xilinx FPGA, perform the following steps:

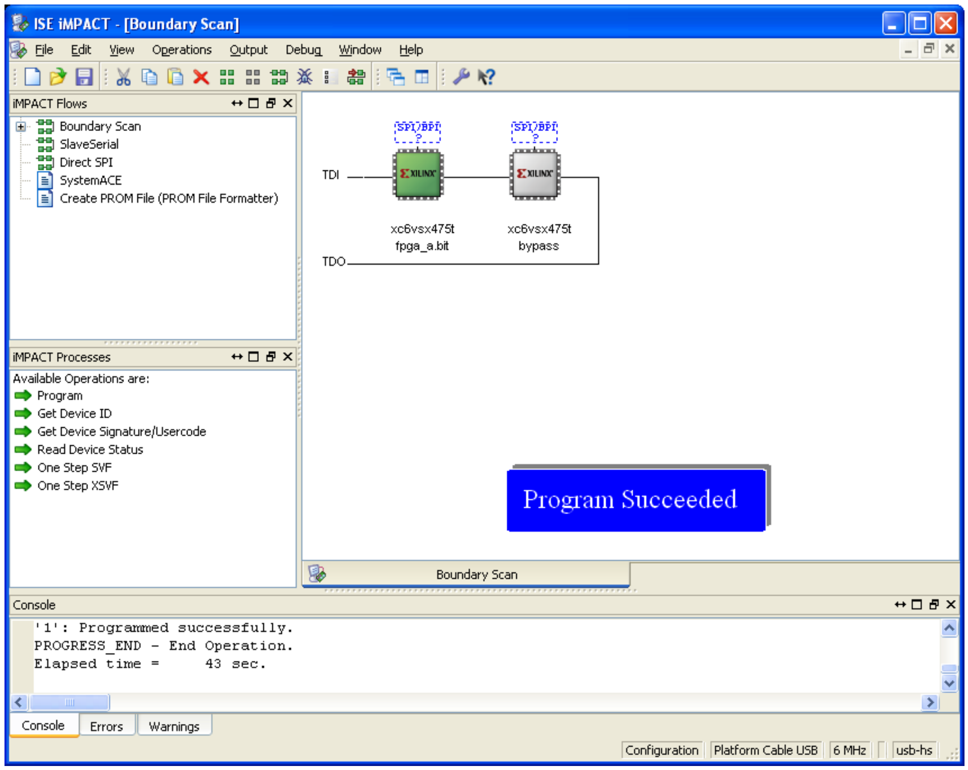
1. Open iMPACT and create a new default project. Select "**Configure devices using Boundary-Scan (JTAG)**" from the iMPACT welcome menu.



2. iMPACT will identify FPGA A and FPGA B (XC6VSX475T – depends on the build option) in the JTAG chain. A pop-up window will display "**Device Programming Properties – Device 1 Programming Properties**". Click "**OK**" to select default options.

3. Right-click on FPGA A and select "**Assign New Configuration File**". Specify the location for the FPGA bit file based on the type of FPGA populated e.g. XC6VSX475T;

4. Right-click on the FPGA and select the "**Program**" option. A "Progress Dialog" box will appear indicating programming progress.



5. Verify that the "FPGAA_DONE" blue LED (DS22 for FPGA A) is enabled, indicating successful configuration of the FPGA.

5 Updating the Marvell MV78200 Software

This section lists detailed instructions for updating/programming the Marvell MV78200 software.

> Note: Minor changes to this procedure may occur over the life of the product, please contact Dini Group for the latest procedures at support@dinigroup.com.

5.1 Setup – Updating the Marvell MV78200 Software

Before updating/programming the Marvell MV78200 software, ensure the following steps have been completed:

1. Attach an ATX Power Supply to the "PCIE PWR" header (J5) on the DN-DUALV6-PCIE-4 Logic Emulation Board.

2. Connect the "Ethernet Cable" to the "ETHERNET" header (J3) on the DN-DUALV6-PCIE-4 Logic Emulation Board. Note: In order to be able to access the board over the network, the network must support DHCP.

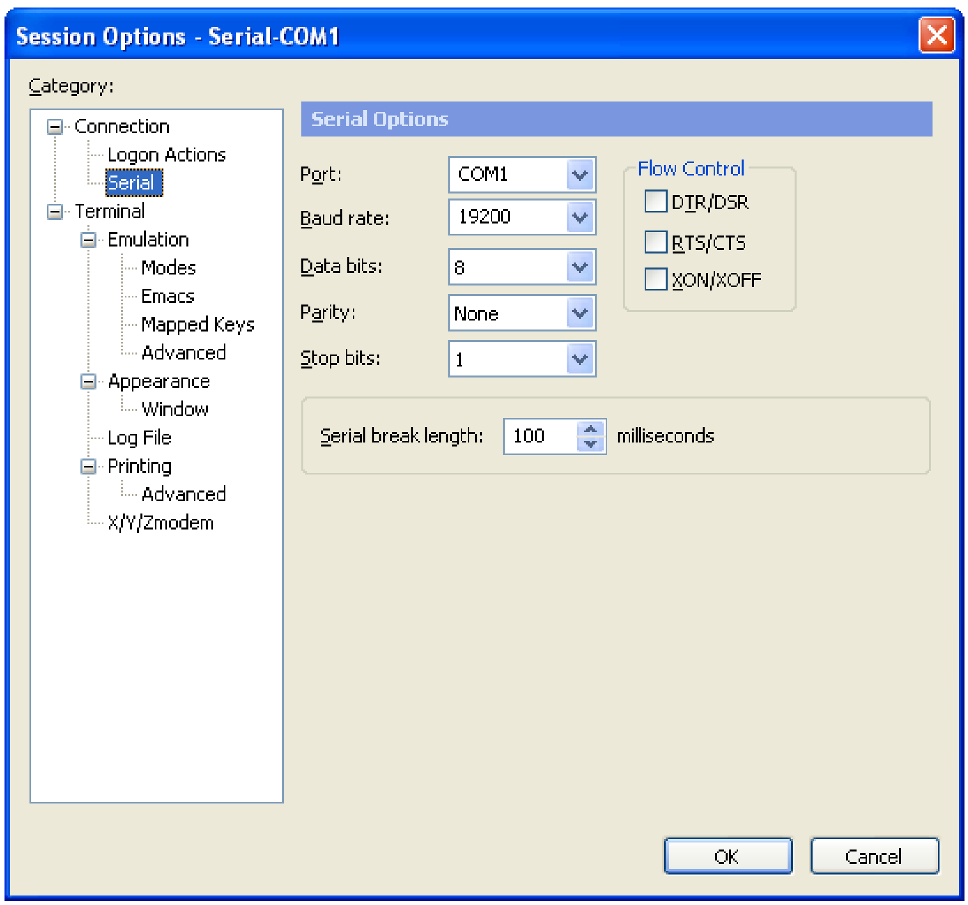
5.2 Powering Up the Board

3. Power up the board by turning ON the ATX power supply and verify the "+12V" LED (DS44) is ON indicating the presence of +12V (located at the right-side of the PCB).

5.3 Open Serial Terminal Session

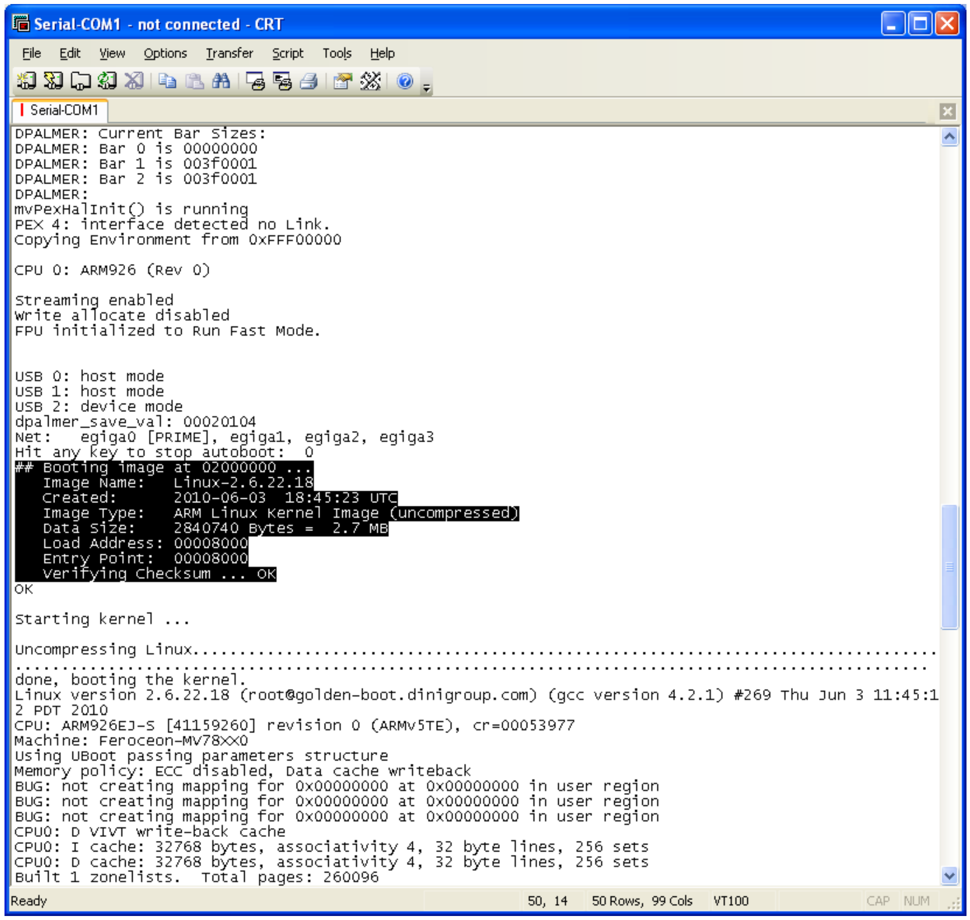
Access to the board is allowed via a Serial Terminal Session.

4. Connect the "RS232 Serial Cable" to the "RS232 CPU" header (J1) on the DN-DUALV6-PCIE-4 Logic Emulation Board. Configure the session as follows:



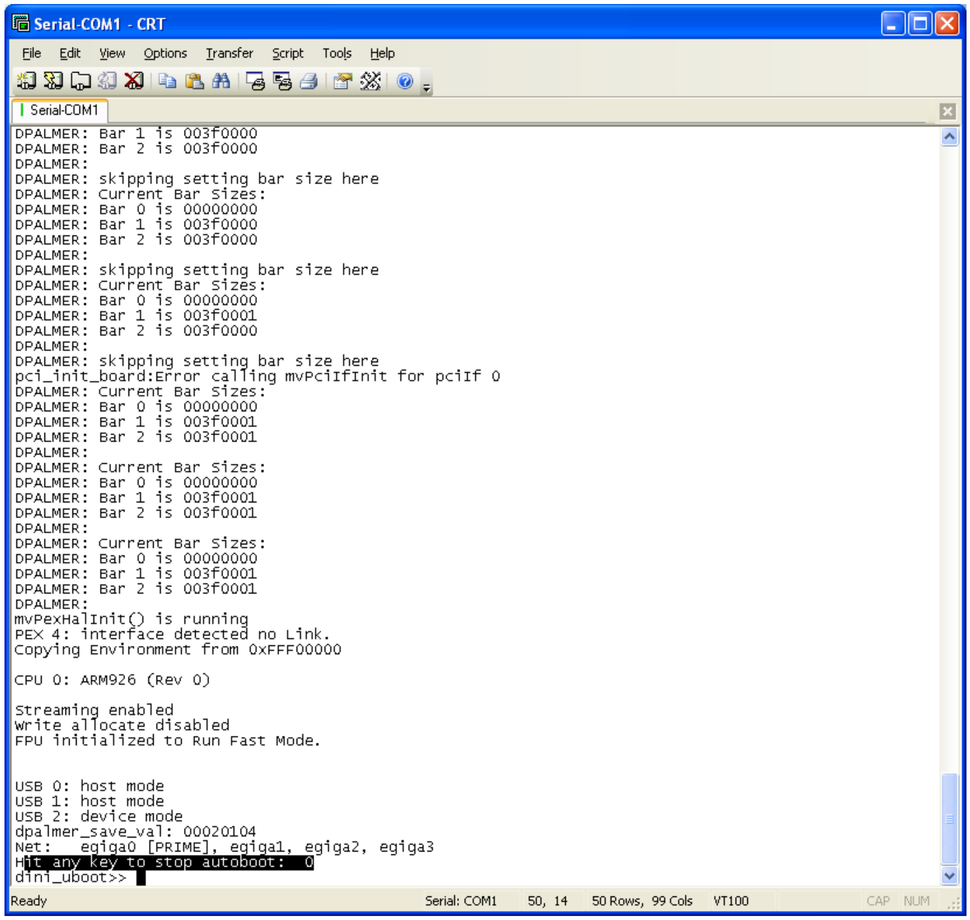
5.4 Verify Linux Kernel Version

5. Power the DN-DUALV6-PCIE-4 Logic Emulation Board and monitor the power-up events in the CRT window. Note: Shortly after power-up, check the Linux Kernel version, as shown in the "Created" date.



5.5 Update the Linux Kernel

6. Power-cycle the DN-DUALV6-PCIE-4 Logic Emulation Board and monitor the power up events in the CRT window. Note: **Press ENTER when the "Hit any key to stop autoboot:**" appears in the CRT window.



7. Enter the following command at the prompt:

   dini_uboot>> protect off 1:0-63

8. Boot into Linux by entering the following command:

   dini_uboot>> boot

9. Once the boot procedure completes, enter the following command:

   -sh-3.2# mount -t tmpfs tmpfs /mnt/ram -o size=32M

10. Enter the following command at the prompt:

    -sh-3.2# cd /mnt/ram

11. Download the update files from the Dini Group website. Place these files on the board (see directory above). Alternatively, if the board is connected to an internet-enabled network, use the "wget" command:

-sh-3.2# wget http://dinigroup.com/~marvellfiles/uImage

Note: If you do not have access to the internet, then you will need to use some other method to transfer files to the board. You can use a USB key, a network mount, or any other linux trick you know.

12. Enter the following command at the prompt:

    sh-3.2# cat uImage > /dev/partition_spi

    Note: This command updates the Linux kernel. If this command fails, the recovery procedure is still possible, but is more complicated.

13. Enter the following command at the prompt:

    sh -sh-3.2# reboot

    Note: It is important to execute the reboot command, and not power-cycling the board. Power cycling may cause the SPI Flash not to get written completely due to write buffering.

5.6 Installing the Root File System (RFS) Update

This procedure will result in the loss of user data on the Linux file system. Back up your data. To check the version number of your root file system, type the following Linux command:

-sh-3.2# cat /root/image.date

14. Power-cycle the DN-DUALV6-PCIE-4 Logic Emulation Board and monitor the power up events in the CRT window. Note: **Press ENTER when the "Hit any key to stop autoboot:**" appears in the CRT window.

15. Enter the following command at the prompt:

    dini_uboot>> run 'spi_boot_recoveryfs'

16. Enter the following command at the prompt:

    -sh-3.2# sh /root/recover.sh

    Note: The recovery process takes about 10 minutes, plus longer for the 180MB download from dinigroup.com.

17. Enter the following command at the prompt:

    sh -sh-3.2# reboot.

Chapter
4

Hardware Description

This chapter describes the hardware features of the DN-DualV6-PCIe-4 Virtex-6 Logic Emulation Board.

1 Description

1.1 Overview

The DN-DualV6-PCIe-4 is a complete logic prototyping system that enables ASIC or IP designers a vehicle to prototype logic and memory designs for a fraction of the cost of existing solutions. A high level block diagram of the DN-DualV6-PCIe-4 Logic Emulation Board is shown in Figure 4, followed by a brief description of each section.

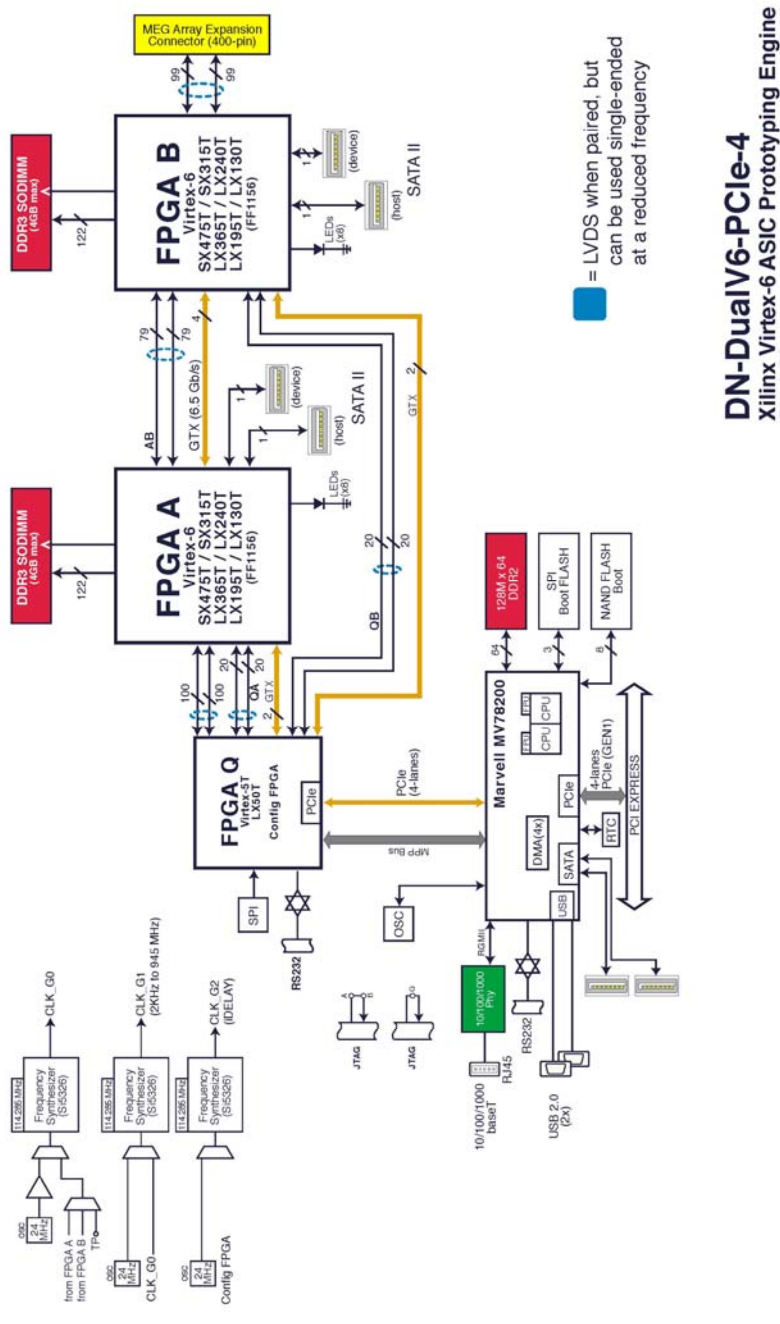


Figure 4 - DN-DualV6-PCIe-4 Logic Emulation Board Block Diagram

The DN-DualV6-PCIe-4 is hosted in a 4-lane PCI Express (GEN1) system but can be used stand-alone and is configured via USB or Ethernet. The FPGA configuration and other miscellaneous board functions are controlled by the Marvell MV78200 CPU. A single DN-DualV6-PCIe-4 configured with two Xilinx Virtex-6 (SX475T) FPGAs can emulate up to 10 million gates of logic as measured by a reasonable ASIC gate counting

standard. This gate count estimate number does not include embedded memories and multipliers resident in each FPGA. One hundred percent (100%) of the Virtex-6 FPGA resources are available to the user.

The DN-DualV6-PCIe-4 provides dual Xilinx Virtex-6 FPGAs in the 1156-pin package. The architecture of the board, maximizes interconnect by providing a number of dedicated busses between the FPGAs, see Figure 4. The Marvell MV78200 CPU in conjunction with the Configuration FPGA (Virtex-5) is used to configure FPGA A/B (Virtex-6) using the SelectMAP configuration mode. JTAG configuration, using the "Xilinx Platform Cable USB" download cable, is provided as an alternate method of configuration and provides an interface to ChipScope and other third party debug tools. The Marvell MV78200 provides a number of high-speed interfaces that are available to the user after configuration. The PCI Express interface between the Marvell 78200 and the Configuration FPGA provides a high-speed data path to the system interface, whether that is USB, Ethernet or PCI Express.

Numerous clocking options exist to allow for a flexible clocking scheme. Three highly configurable clock multipliers (Si5326) provide global clock networks. External memory to the Virtex-6 FPGAs is realized using a 64 bit, 204 pin SODIMM that accepts PC3-8500 DDR3 SODIMMs. One 400 pin MEG-Array connector on the bottom of the printed circuit board assembly (PCBA) is used to interface to other Dini Group products, e.g. DNMEG_Obs Daughter Card.

In standalone mode, the DN-DualV6-PCIe-4 receives power from an external +12V ATX power supply. An RS232 interface exists to allow communication with the application. LEDs are used to indicate configuration status, power supply presence and numerous LEDs are provided for the user.

1 Marvell MV78200 CPU

1.1 Overview

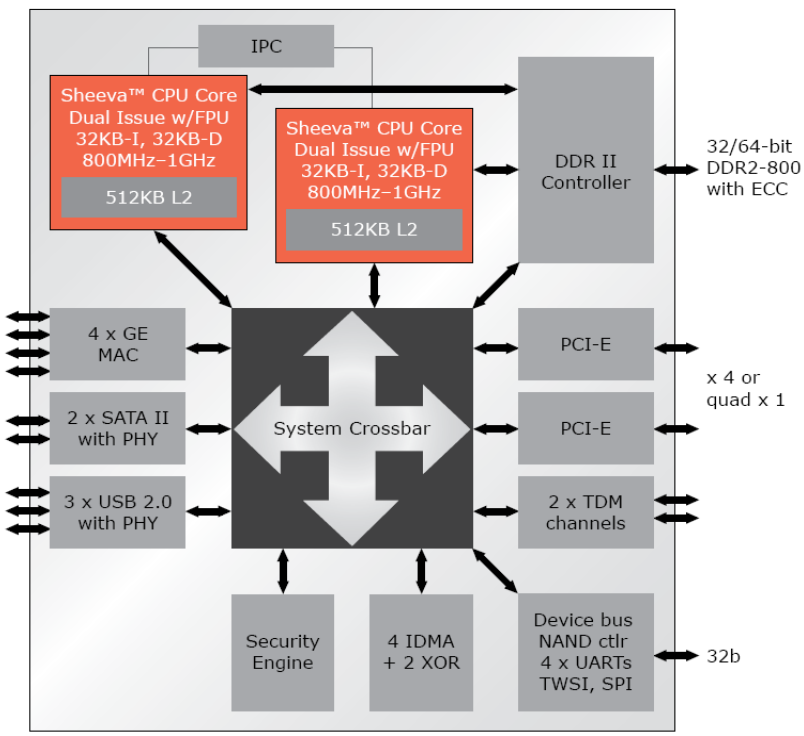
The Marvell MV78200 is a dual-core, high-performance, low-power, highly integrated processor with Marvell's Sheeva™ ARMv5TE-compliant CPU core. Built on Marvell's innovative Discovery™ system controller platform, the MV78200 is a complete system-on-chip (SoC) solution. Optimized for low power operation, the MV78200 is ideally suited to a wide range of applications ranging from sophisticated routers, switches and wireless base stations to high-volume laser printers applications.

The MV78200 offers unparalleled integration that makes system design simple and cost efficient. The SoC integrates:

- High-performance dual-issue CPU with Vector Floating Point (VFP) support
- 800 MHz and 1 Ghz operating speed

- 32KB-Instruction and 32KB-Data 4-way, set-associative L1 cache per core
- 512KB unified 8-way, set-associative L2 cache per core
- 40/72-bit high bandwidth DDR2 memory interface (up to 800 MHz data rate)
- Four Gigabit Ethernet MACs with interface options
- Two PCI-Express ports (x4 or Quad x1)
- Three USB 2.0 ports with integrated PHYs
- Two SATA 2.0 ports with integrated PHYs
- Security engine
- Pin-compatible with single-core (MV78100) version.

The innovative, on-chip crossbar architecture with any-to-any connectivity enables concurrent transactions among multiple units that results in high system throughput allowing system designers to create high-performance scalable systems.



1.2 Reset Strapping Options

Internal pull-up/down resistors set the default mode of operation of the Marvell MV87200 CPU. External pull-up/down resistors are required to change the default mode of operation. These signals must remain pulled up or down until SYSRSTn de-

assertion (zero hold time in respect to SYSRSTn de-assertion). See Table 2 for the default board configuration.

Table 2 - Reset Strapping Options

Configuration Mode	Configuration Resistors	
	Installed	Not Installed
DEV_D[0] Reserved NOTE: Internally pulled down to 0x0.	R515	R81
DEV_D[1] Reserved NOTE: Internally pulled down to 0x0.	R38	R28
DEV_D[2] PCI Express port0 mode select ***0 = Endpoint** 1 = Root Complex NOTE: Internally pulled up to 0x1.	R521	R80
DEV_D[3] PCI Express port0 configuration ***0 = x4** 1 = Quad x1 NOTE: Internally pulled down to 0x0.	R527	R88
DEV_D[4] PCI Express port1 configuration ***0 = x4** 1 = Quad x1 NOTE: Internally pulled up to 0x1.	R50	R51
DEV_D[7:5] HCLK Frequency select 0x0 = 167 MHz 0x0 = Reserved ***0x1 = 200 MHz** 0x2 = 267 MHz 0x3 = 333 MHz 0x4 = 400 MHz 0x5 = 250 MHz 0x6 = 300 MHz 0x7 = Reserved NOTE: Internally pulled to 0x2.	R45, R526, R531	R26, R87, R90
DEV_D[11:8] PCLK0 to HCLK ratio 0x0 = 1 0x1 = 1.5 0x2 = 2	R505, R494, R435, R504	R506, R493, R53, R503

Configuration Mode	Configuration Resistors	
	Installed	Not Installed
***0x3 = 2.5** 0x4 = 3 0x5 = 3.5 0x6 = 4 0x7 = 4.5 0x8 = 5 0x9 = 5.5 0xA = 6 0xB - 0xF = Reserved NOTE: Internally pulled to 0x4.		
DEV_D[13:12] CPU0 L2 to PCLK0 ratio 0x0 = 1 ***0x1 = 2** 0x2 = 3 0x3 = Reserved NOTE: Internally pulled to 0x1.	R54, R57	R436, R437
DEV_D[17:14] PCLK1 to HCLK ratio 0x0 = 1 0x1 = 1.5 0x2 = 2 ***0x3 = 2.5** 0x4 = 3 0x5 = 3.5 0x6 = 4 0x7 = 4.5 0x8 = 5 0x9 = 5.5 0xA = 6 0xB - 0xF = Reserved NOTE: Internally pulled to 0x4.	R75, R74, R496, R52	R479, R478, R495, R433
DEV_D[19:18] CPU1 L2 to PCLK1 ratio 0x0 = 1 ***0x1 = 2** 0x2 = 3 0x3 = Reserved	R459, R490	R64, R489

Configuration Mode	Configuration Resistors	
	Installed	Not Installed
NOTE: Internally pulled to 0x1.		
DEV_D[20] CPU1 Enable 0 = Disable ***1 = Enable** NOTE: Internally pulled down to 0x0.	R78	R486
DEV_D[22:21] DEV_BootCEn Device Width ***00 = 8 bits** 01 = 16 bits 10 = 32 bits 11 = Reserved NOTE: Internally pulled down to 0x0.	R491, R39	R492, R40
DEV_D[24:23] Boot From NAND Flash Defines the default value of bit <NFBoot> in the NAND Flash Control Register 0x0 = Boot from device bus (NOR Flash, ROM ...) ***0x1 = Boot from SPI** 0x2 = Boot from CE don't care NAND Flash 0x3 = Boot from CE care NAND Flash NOTE: Internally pulled down to 0x0.	R498. R487	R497, R488
DEV_D[26:25] NAND Flash Initialization Sequence ***0x0 = No initialization** 0x1 = Init sequence enabled, 3 address cycles 0x2 = Init sequence enabled, 4 address cycles 0x3 = Init sequence enabled, 5 address cycles NOTE: Internally pulled down to 0x0.	R500, R501	R499, R502
DEV_D[27] Big Endian initialization ***0 = Little Endian** 1 = Big Endian NOTE: Internally pulled down to 0x0.	R25	R360
DEV_D[28] CLK25 Select 0 = Both CLK25_PT and CLK25_SSC are used ***1 = Only CLK25_PT is used** NOTE: Internally pulled up to 0x1.	R361	R34
DEV_D[29] DRAM Interface Width ***0 = 64b/72b**	R33	R390

Configuration Mode	Configuration Resistors	
	Installed	Not Installed
1 = 32b/40b NOTE: Internally pulled to 0x0.		
DEV_D[30] Nand flash initialization command ***0 = Append command 0x30** 1 = Do not append command 0x30 NOTE: Internally pulled to 0x0.	R37	R394
DEV_D[31] VDDO_C Voltage Select ***0 = 1.8V** 1 = 3.3V NOTE: Internally pulled down to 0x1.	R23	R355
DEV_ALE[0] VDDO_B Voltage Select ***0 = 1.8V** 1 = 3.3V NOTE: Internally pulled up to 0x1.	R41	R427
DEV_ALE[1] VDDO_D Voltage Select ***0 = 1.8V** 1 = 3.3V NOTE: Internally pulled up to 0x1.	R70	R467
DEV_WEn[0] VDD_GE Voltage Select ***0 = 1.8V** 1 = 3.3V NOTE: Internally pulled up to 0x0.	R507	R508
DEV_WEn[1] DEV_WEn and DEV_OEn multiplexing option for A[16:15] bits ***0 - A[16:15] bits are not multiplexed on OE and WE signals.** 1 - A[16:15] bits are multiplexed on OE and WE signals NOTE: Internally pulled down to 0x0.	R510	R509
DEV_WEn[2] Reserved (ATE) NOTE: Internally pulled down to 0x0.	R511	R512
DEV_WEn[3] Reserved (TW) NOTE: Internally pulled down to 0x0.	R58	R440
DEV_A[0] TCLK Mode Select 0 = TCLK is driven from TCLK_IN input ***1 = TCLK generated internally by TCLK PLL** NOTE: Internally pulled up to 0x1.	R468	R68

Configuration Mode	Configuration Resistors	
	Installed	Not Installed
DEV_A[2:1] TCLK frequency select/TCLK De-skew PLL Tune If DEV_A[0] is set to 1 - DEV_A[2:1] functions as TCLK frequency select: ***0x0 = 166MHz** 0x1 = 200MHz 0x2, 0x3 = Reserved If DEV_A[0] is set to 0 - DEV_A[1:1] functions as TCLK De-skew PLL Tune. Setting recommendation will be released after chip tape out. NOTE: Internally pulled to 0x1.	R65, R56	R452, R439
GE0_TXD[0] TCLK De-skewer PLL Frequency Band Functions as TCLK De-Skewer PLL Frequency band Select. Relevant for De-skew mode only (DEV_A[0] is set to 0] ***0=166 MHz** 1=200MHz NOTE: Internally pulled down to 0x0.	R24	R359
GE0_TXD[1] Reserved NOTE: Internally pulled down to 0x1.	R380	R32
GE0_TXD[3:2] DEV_ALE Mode Select ***0x0 = Address 2. ALE 1 TCLK cycle** 0x1 = Address 3. ALE 2 TCLK cycle 0x2 = Address 4. ALE 3 TCLK cycle 0x3 = Reserved NOTE: Internally pulled down to 0x0.	R35, R36	R388, R393

1.3 Boot Options

The Marvell MV78200 dual CPU implementation assumes that the CPU0 boots first, completes the proper chip and system configuration settings, and then enables CPU1 boot. Upon reset de-assertion, CPU0 starts its boot from the DEV_CSn. As part of its boot code, CPU0 sets all the MV78200 configuration registers, initializes the DRAM, wakes up the PCI Express link, and sets the different chip interface address map. It also sets the CPU address decoding windows, enabling CPU1 to boot from a different boot device. CPU0 then clears CPU1's <CPUReset> field in the CPU Control and Status Register, thereby enabling CPU1 to start booting. Two boot options are provided on the DN-DualV6-PCIe-4.

1.3.1 Booting from SPI Flash

Device Bus, DEV_AD[24:23] = 0x1 selects the "Boot from SPI" on the Marvell MV78200 CPU. A general purpose SPI interface is provided. The M25P64 (U41), is a 64 Mbit (8M x 8) Serial Flash Memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus instructions allowing clock frequency up to 50 MHz (TCLK/4), see Figure 5. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

An enhanced Fast Program/Erase mode is available to speed up operations in factory environment. The device enters this mode whenever the VPPH voltage is applied to the Write Protect/Enhanced Program Supply Voltage pin (W/VPP). The memory is organized as 128 sectors, each containing 256 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 32768 pages, or 8388608 bytes.

The whole memory can be erased using the Bulk Erase instruction, or a sector at a time, using the Sector Erase instruction.

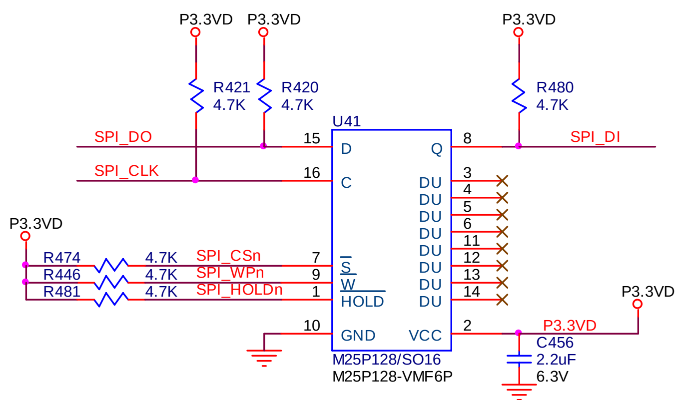


Figure 5 - SPI Flash Boot

The SPI Flash can be programmed by an "In System Programming" programmer e.g DediProg SF100. A programming header is provided on the board, see Table 3.

Table 3 – SPI Flash Programming Interface

Signal Name	SPI Flash	SPI Flash Header
SPI_CLK	U41-16	J22-5
SPI_CSn	U41-7	J22-1
SPI_DO	U41-15	J22-3
SPI_DI	U41-8	J22-2

1.3.2 Booting from NAND Flash

Device Bus, DEV_AD[24:23] = 0x2 selects the "Boot from CE don't care NAND Flash" on the Marvell MV78200 CPU. The Marvell MV78200 CPU supports booting from NAND Flash when the fist block is placed on 00h block address, and is guaranteed to be a valid block with no errors, see *MV-S800598-00C - Functional Specifications* for more information.

The NAND02G-B2C (U11) Flash, is a non-volatile Flash memory that uses NAND cell technology, see Figure 6. The device is 2 Gbits and operates from a 1.8V voltage supply. The size of a Page is 2112 Bytes (2048 + 64 spare) and is configured as an x8 bus width. The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 Input/Output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

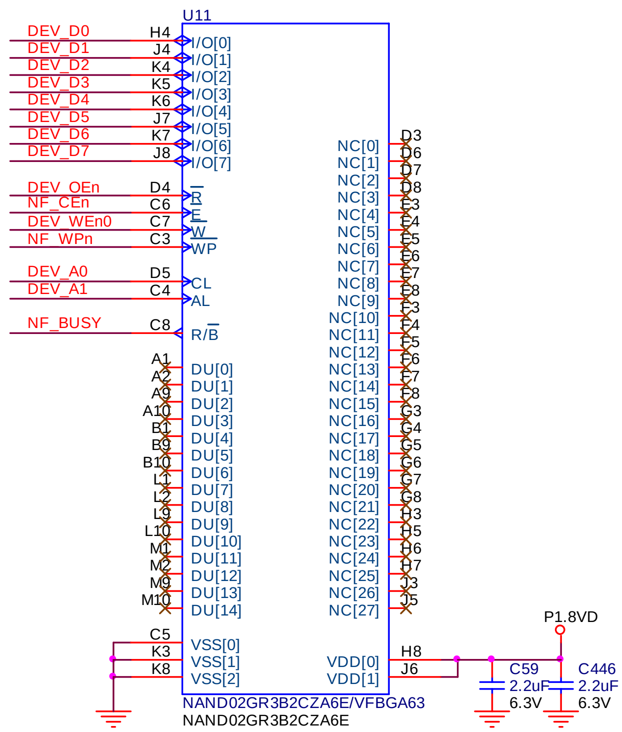


Figure 6 - NAND Flash 2Gbit (CE Don't Care)

Each block can be programmed and erased over 100,000 cycles. To extend the lifetime of NAND Flash devices it is strongly recommended to implement an Error Correction Code (ECC). The device feature a Write Protect pin (pulled high by R66) that allows performing hardware protection against program and erase operations.

The device feature an open-drain Ready/Busy output that can be used to identify if the Program/Erase/Read (P/E/R) Controller is currently active. The use of an open-drain

output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor.

The device has a Chip Enable Don't Care feature, which allows code to be directly downloaded by the CPU, as Chip Enable transitions during the latency time do not stop the read operation.

The NAND Flash is connected to the Device Bus on the Marvell CPU, see Table 4. The NAND Flash is also connected the Configuration FPGA, see the schematic for further details. This allows the NAND Flash to be programmed via the Configuration FPGA.

Table 4 – NAND Flash Device Bus Interface

Signal Name	NAND Flash	CPU
DEV_D0	U11-H4	U4-U25
DEV_D1	U11-J4	U4-U26
DEV_D2	U11-K4	U4-T24
DEV_D3	U11-K5	U4-T26
DEV_D4	U11-K6	U4-R21
DEV_D5	U11-J7	U4-R22
DEV_D6	U11-K7	U4-R23
DEV_D7	U11-J8	U4-R24
DEV_OEn	U11-D4	U4-21
NF_CEn	U11-C6	U4-U21
DEV_WEn0	U11-C7	U4-AA23
NF_WPn	U11-C3	Pull-up (R66)
DEV_A0	U11-D5	U4-U22
DEV_A1	U11-C4	U4-U23
NF_BUSY	U11-C8	LED (DS8)

1.4 CPU Memory (DDR2)

The Marvell MV78200 CPU interface to four DDR2 SDRAM (128M x 16) devices via a 64-bit bus M_DQ[63..0], see Figure 7. The DDR2 SDRAM (MT47H128M16HG) uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4n-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the DDR2 SDRAM effectively consists of a single 4n-bit-wide, one clock- cycle data transfer at the internal DRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O balls. A bidirectional data strobe (DQS, DQS#) is

transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

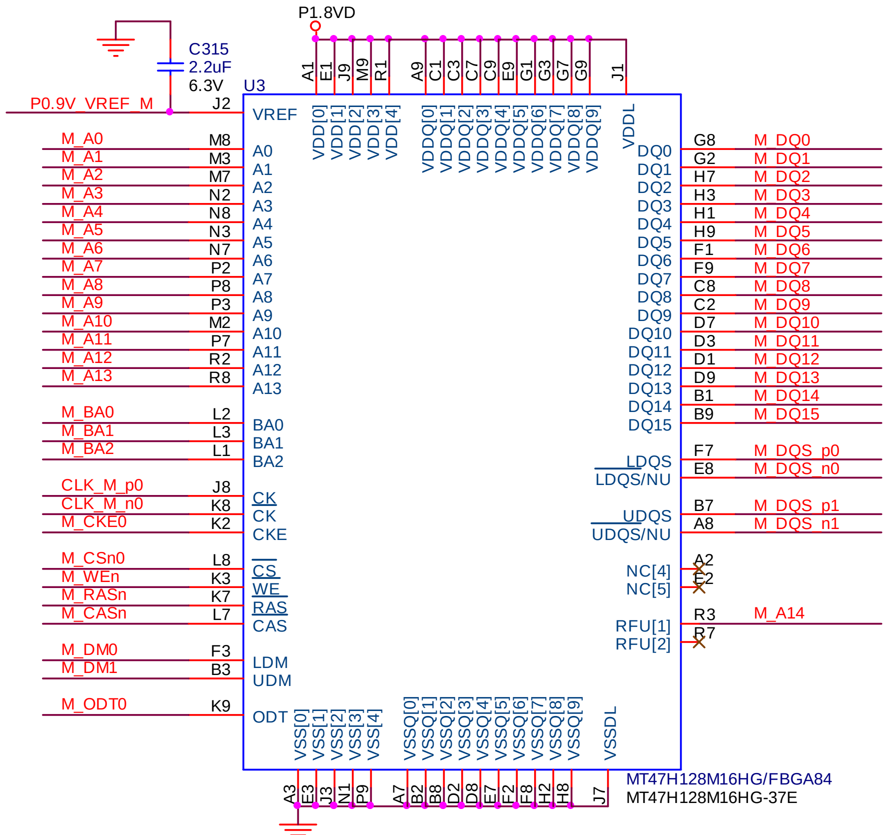


Figure 7 – CPU Memory - DDR2 SDRAM (128M x 64)

The DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS as well as to both edges of CK.

1.5 PCI Express Interface

The Marvell MV78200 has two PCI Express interfaces, Port 0 and Port 1. PCI Express Port 0 is configured as an Endpoint (DEV_AD[2] = 0), while PCI Express Port 1 is always a Root Complex. The PCI Express ports are PCI Express Base 1.1 compliant and runs at 2.5GHz allowing for 2Gb/s of bandwidth in each direction. The PCI Express port uses 64-bit addressing, as a master or target. It supports extended PCI Express configuration space, advanced error reporting, power management, L0s and

software L1, interrupt emulation message, and error messages. The device also support P2P bridging (non-transparent bridge) between PEX0 and PEX1 ports, see *MV-S800598-00C - Functional Specifications* for more information.

1.5.1 PCI Express Port 0

Port 0 is configured as an Endpoint (DEV_AD[2] = 0). PEX0_T/R_p[0..3] is routed as differential (LVDS) traces, AC-coupled, and connected to the PCI Express Fingers, see Table 5.

Table 5 – PCI Express Port 0 Interconnect

Signal Name	CPU	PCI Express Edge Connector
PEX0_T_P0	U4-AE2	P1-A16
PEX0_T_N0	U4-AF2	P1-A17
PEX0_T_P1	U4-AE4	P1-A21
PEX0_T_N1	U4-AF3	P1-A22
PEX0_T_P2	U4-AE3	P1-A25
PEX0_T_N2	U4-AF4	P1-A26
PEX0_T_P3	U4-AE5	P1-A29
PEX0_T_N3	U4-AF5	P1-A30
PEX0_R_P0	U4-AC3	P1-B14
PEX0_R_N0	U4-AB3	P1-B15
PEX0_R_P1	U4-AB4	P1-B19
PEX0_R_N1	U4-AA4	P1-B20
PEX0_R_P2	U4-AC5	P1-B23
PEX0_R_N2	U4-AB5	P1-B24
PEX0_R_P3	U4-AB6	P1-B27
PEX0_R_N3	U4-AA6	P1-B28

1.5.2 PCI Express Port 1

PCI Express Port 1 is always a Root Complex. PEX1_T/R_p[0..3] is routed as differential (LVDS) traces, AC-coupled, and connected to the Configuration FPGA, see Table 6.

Table 6 – PCI Express Port 1 Interconnect

Signal Name	CPU	Configuration FPGA
PEX1_T_P0	U4-AE10	U17-G1

Signal Name	CPU	Configuration FPGA
PEX1_T_N0	U4-AF10	U17-H1
PEX1_T_P1	U4-AE9	U17-K1
PEX1_T_N1	U4-AF9	U17-J1
PEX1_T_P2	U4-AE8	U17-N1
PEX1_T_N2	U4-AF8	U17-P1
PEX1_T_P3	U4-AE7	U17-T1
PEX1_T_N3	U4-AF7	U17-R1
PEX1_R_P0	U4-AB11	U17-F2
PEX1_R_N0	U4-AC11	U17-G2
PEX1_R_P1	U4-AA10	U17-L2
PEX1_R_N1	U4-AB10	U17-K2
PEX1_R_P2	U4-AB9	U17-M2
PEX1_R_N2	U4-AC9	U17-N2
PEX1_R_P3	U4-AA8	U17-U2
PEX1_R_N3	U4-AB8	U17-T2

1.5.3 PCI Express Clocking

Refer to the PCI Express Reference Clocks section of this manual.

1.6 USB Interface

The Marvell MV78200 integrates three USB2.0 compliant ports, including integrated PHYs. Each USB 2.0 interface contains a single dual-role controller that can act as a host or a peripheral controller. USB0 (J2) is configured as a Host, used during Stand-alone configuration with a USB Flash Drive. USB2 (J4) is configured as a Device and is used during Stand-alone configuration to interface the EMU GUI. The USB ports have a dedicated DMA for data transfer between memory and port.

The USB signals are routed as differential traces and connect to the Marvell MV78200 via common mode filters (T1/T2), see Table 7.

Table 7 – USB Interconnect

Signal Name	CPU	USB
USB_D_p0	U4-AE13	J2-3
USB_D_n0	U4-AF13	J2-2
USB_D_p2	U4-AB13	J4-3
USB_D_n2	U4-AC13	J4-2

The NUP2201MR6 (D4/D5) transient voltage suppressors are designed to protect the high speed data lines from ESD. The AP2171 (U29) is an integrated high-side power switches optimized for Universal Serial Bus (USB) and other hot-swap applications.

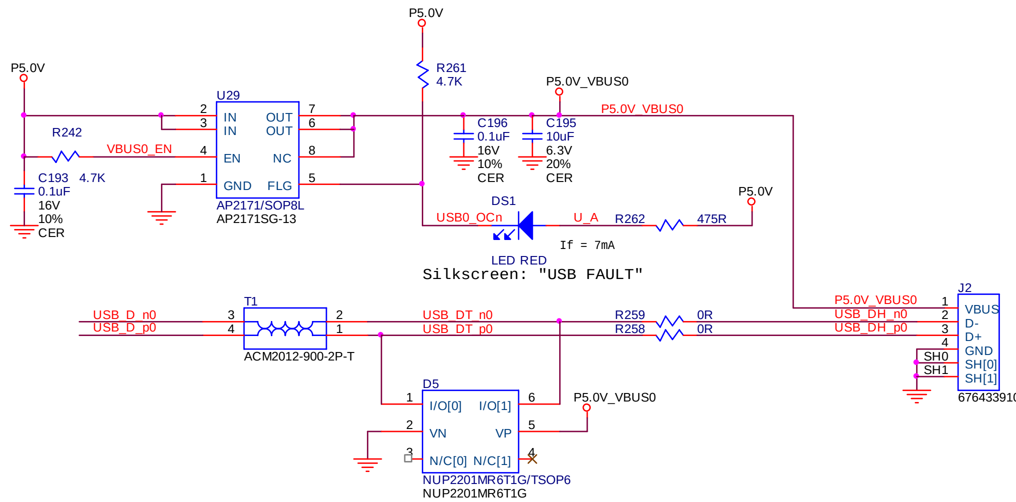


Figure 8 - USB2.0 (Port 0) Host (Type A)

The AP2171 offer current (1.5A) and thermal limiting and short circuit protection as well as controlled rise time and under-voltage lockout functionality.

1.7 Gigabit Ethernet Interface

The Gigabit Ethernet Port (GbE) includes an IEEE802.3 compliant 10/100/1000Mb MAC. The Alaska 88E1116R (U1) Gigabit Ethernet Transceiver is a physical layer device (PHY) between the Marvell MV78200 and the Ethernet connector (J3). The 88E111R device supports the Reduced pin count for GMII (RGMII) for direct connection to the Marvell MV78200.

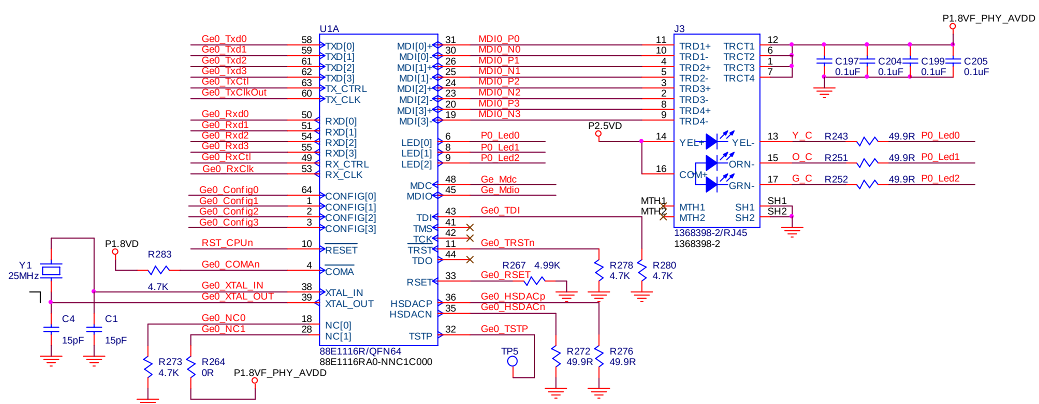


Figure 9 - 10/100/1000 Ethernet (RGMII)

The 1368398-2 (J3) is a Gigabit Ethernet single port jack (RJ45) with integrated magnetics and LEDs, see Figure 9.

1.8 SATA Interface

Serial ATA is a high-speed serial link replacement for the parallel ATA attachment of mass storage devices. The serial link employed is a high-speed differential layer that utilizes gigabit technology and 8b/10b encoding. The Marvell MV78200 includes two SATA II compliant ports. The device employs the latest SATA II PHY technology, with 3.0Gbps (Gen2i) and backwards compatible with 1.5 Gbps (Gen1i) SATA I, see Figure 10. Both TX/RX signal pairs are differentially routed and AC-coupled with 0.1uF capacitors.

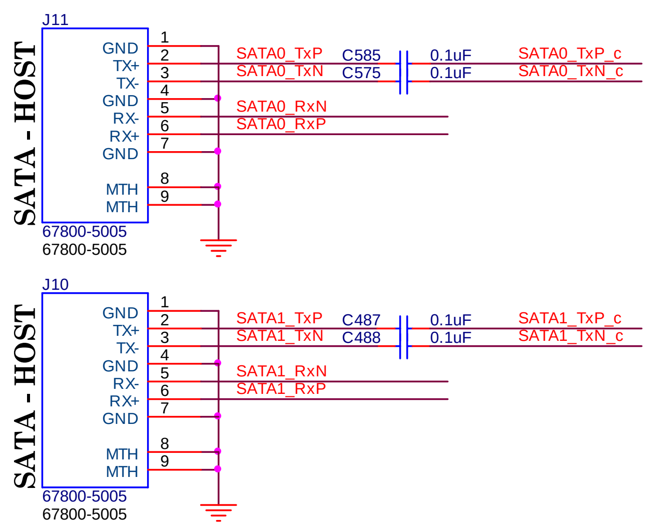


Figure 10 - SATA Interface

The two SATA II ports connects directly to the Marvell MV78200, see Table 8.

Table 8 – SATA II CPU Interconnect

Signal Name	CPU	SATA
SA0_TXP	U4.R1	J11.2
SA0_TXN	U4.R2	J11.3
SA0_RXP	U4.U2	J11.6
SA0_RXN	U4.U1	J11.5
SA1_TXP	U4.R4	J10.2
SA1_TXN	U4.R5	J10.3
SA1_RXP	U4.U5	J10.6
SA1_RXN	U4.U4	J10.5

1.9 UART (RS232) Interface

See RS232 Port section in this user manual.

1.10 Real Time Clock

The DS1338 (U36) serial real-time clock (RTC) is a low-power, full binary-coded decimal (BCD) clock/calendar plus 56 bytes of NV SRAM. Address and data are transferred serially through an I^2C interface. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The RTC is connected to the Two Wire Serial Interface (TWSI) port 1, see Figure 11 and mapped to address 0x68h.

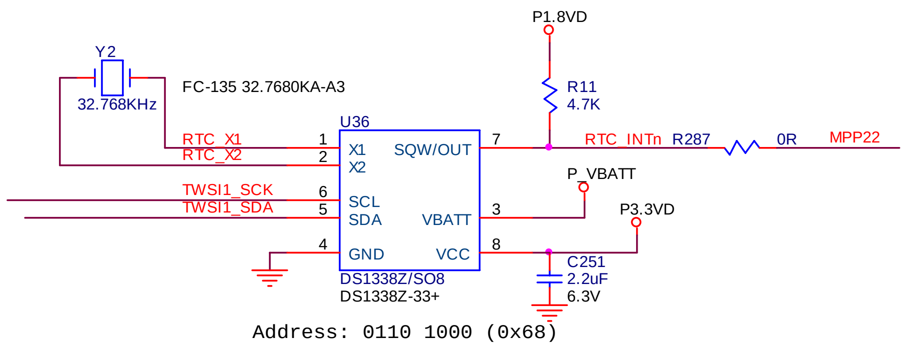


Figure 11 - Real Time Clock (RTC)

The TWSI master starts a transaction by driving a start condition, followed by a 7-bit slave address and a read/write bit indication. The target TWSI slave responds with an acknowledge etc. In addition to the RTC, the CPU Temperature Monitor (U37) and an EEPROM (U32) is connected to the TWSI1 bus, please see schematic for more information.

1.11 Temperature Monitor

The MAX1617A is a precise digital thermometer that reports the temperature of both a remote sensor and its own package. The remote sensor is a diode-connected transistor—typically a low-cost, easily mounted 2N3904 NPN type—that replaces conventional thermistors or thermocouples. Remote accuracy is ±3°C for multiple transistor manufacturers, with no calibration needed. The remote channel can also measure the die temperature of other ICs, such as microprocessors, that contain an on-chip, diode-connected transistor. The Marvell MV78200 is connected to a temperature sensor (U37) via the TWSI1 serial bus. This sensor measures is mapped to address 0x4Ch, see Figure 12. The maximum recommended operating temperature of the CPU is 85 degrees. When the CPU measures the temperature above 80 degrees, it will immediately RESET the CPU.

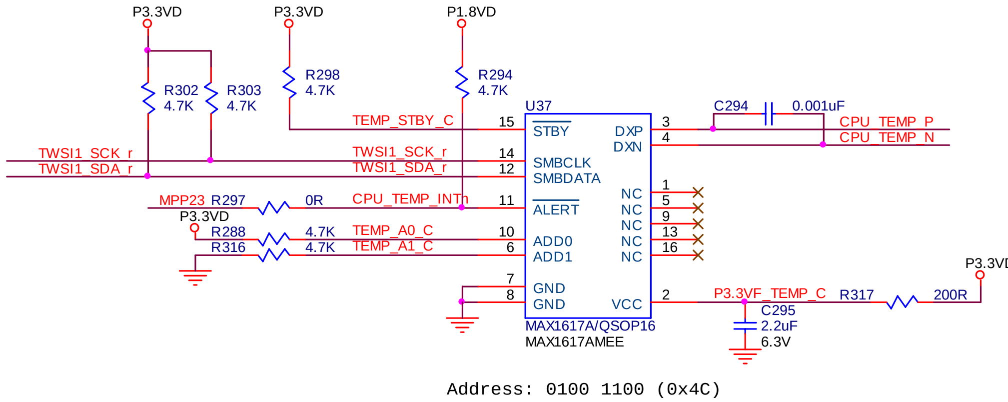


Figure 12 – CPU Temperature Sensor

The connection between the Marvell MV78200 and the Temperature Sensor are shown in Table 9.

Table 9 - Connection between Marvell MV78200 and Temperature Sensor

Signal Name	Temp Sensor	CPU
CPU_TEMP_P	U37-3	U4-P12
CPU_TEMP_N	U37-4	U4-N13

1.12 JTAG Boundary-Scan (JTAG) Interface

The Marvell MV78200 JTAG interface is used for chip boundary scan as well as for CPU cores debugger. The two CPU core TAP controllers are chained (CPU0_TDO is connected to CPU1_TDI; CPU1_TDO is driven on J_TDO pin). Figure 13 shows J23, the JTAG connector used to debug the Marvell MV78200.

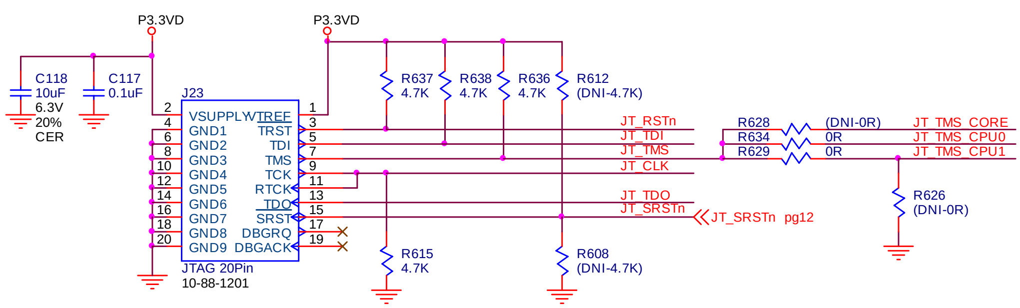


Figure 13 - CPU JTAG Connector

Table 10 shows the connection between the CPU JTAG connector and the Marvell MV78200.

Table 10 – CPU TAG connection to the Marvell MV 78200

Signal Name	JTAG Connector	CPU
JT_CLK	J23-9	U4-M5
JT_TDI	J23-5	U4-M4
JT_TDO	J23-13	U4-K4
JT_TMS_CORE	J23-7	U4-J5
JT_TMS_CPU0	J23-7	U4-K5
JT_TMS_CPU1	J23-7	U4-K6
JT_RSTn	J23-3	U4-M6
JT_SRSTn	J23-15	R336

2 Configuration FPGA (Virtex-5)

2.1 Overview

The Virtex-5 family provides the newest most powerful features in the FPGA market. Using the second generation ASMBL™ (Advanced Silicon Modular Block) column-based architecture, the Virtex-5 family contains five distinct platforms (sub-families), the most choice offered by any FPGA family. Each platform contains a different ratio of features to address the needs of a wide variety of advanced logic designs. In addition to the most advanced, high-performance logic fabric, Virtex-5 FPGAs contain many hard-IP system level blocks, including powerful 36-Kbit block RAM/FIFOs, second generation 25 x 18 DSP slices, SelectIO™ technology with built-in digitally controlled impedance, ChipSync™ source-synchronous interface blocks, system monitor functionality, enhanced clock management tiles with integrated DCM (Digital Clock Managers) and phase-locked-loop (PLL) clock generators, and advanced configuration options. Additional platform dependant features include power-optimized high-speed serial transceiver blocks for enhanced serial connectivity, PCI Express® compliant integrated Endpoint blocks, tri-mode Ethernet MACs (Media Access Controllers), and high-performance PowerPC® 440 microprocessor embedded blocks. These features allow advanced logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 65-nm state-of-the-art copper process technology, Virtex-5 FPGAs are a programmable alternative to custom ASIC technology. Most advanced system designs require the programmable strength of FPGAs. Virtex-5 FPGAs offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP, hard/soft microprocessor, and connectivity capabilities. The Virtex-5 LXT, SXT, TXT, and FXT platforms include advanced high-speed serial connectivity and link/transaction layer capability. For more information, please reference the Xilinx Virtex-5 literature.

2.2 Summary of Virtex-5 FPGA Features

- Five platforms LX, LXT, SXT, TXT, and FXT
  - Virtex-5 LX: High-performance general logic applications
  - Virtex-5 LXT: High-performance logic with advanced serial connectivity
  - Virtex-5 SXT: High-performance signal processing applications with advanced serial connectivity
  - Virtex-5 TXT: High-performance systems with double density advanced serial connectivity
  - Virtex-5 FXT: High-performance embedded systems with advanced serial connectivity
- Cross-platform compatibility
  - LXT, SXT, and FXT devices are footprint compatible in the same package using adjustable voltage regulators
- Most advanced, high-performance, optimal-utilization,
- FPGA fabric
  - Real 6-input look-up table (LUT) technology
  - Dual 5-LUT option
  - Improved reduced-hop routing
  - 64-bit distributed RAM option
  - SRL32/Dual SRL16 option
- Powerful clock management tile (CMT) clocking
  - Digital Clock Manager (DCM) blocks for zero delay buffering, frequency synthesis, and clock phase shifting
  - PLL blocks for input jitter filtering, zero delay buffering, frequency synthesis, and phase-matched clock division
- 36-Kbit block RAM/FIFOs
  - True dual-port RAM blocks
  - Enhanced optional programmable FIFO logic
  - Programmable
  - True dual-port widths up to x36
  - Simple dual-port widths up to x72
  - Built-in optional error-correction circuitry
  - Optionally program each block as two independent 18-Kbit blocks
- High-performance parallel SelectIO technology
  - 1.2 to 3.3V I/O Operation
  - Source-synchronous interfacing using ChipSync™ technology

    - Digitally-controlled impedance (DCI) active termination
    - Flexible fine-grained I/O banking
    - High-speed memory interface support
- Advanced DSP48E slices
    - 25 x 18, two's complement, multiplication
    - Optional adder, subtracter, and accumulator
    - Optional pipelining
    - Optional bitwise logical functionality
    - Dedicated cascade connections
- Flexible configuration options
    - SPI and Parallel FLASH interface
    - Multi-bitstream support with dedicated fallback reconfiguration logic
    - Auto bus width detection capability
- System Monitoring capability on all devices
    - On-chip/Off-chip thermal monitoring
    - On-chip/Off-chip power supply monitoring
    - JTAG access to all monitored quantities
- Integrated Endpoint blocks for PCI Express Designs
    - LXT, SXT, TXT, and FXT Platforms
    - Compliant with the PCI Express Base Specification 1.1
    - x1, x4, or x8 lane support per block
    - Works in conjunction with RocketIO™ transceivers
- Tri-mode 10/100/1000 Mb/s Ethernet MACs
    - LXT, SXT, TXT, and FXT Platforms
    - RocketIO transceivers can be used as PHY or connect to external PHY using many soft MII (Media Independent Interface) options
- RocketIO GTP transceivers 100 Mb/s to 3.75 Gb/s
    - LXT and SXT Platforms
- RocketIO GTX transceivers 150 Mb/s to 6.5 Gb/s
- TXT and FXT Platforms
- PowerPC 440 Microprocessors
    - FXT Platform only
    - RISC architecture
    - 7-stage pipeline
    - 32-Kbyte instruction and data caches included
    - Optimized processor interface structure (crossbar)

- 65-nm copper CMOS process technology
- 1.0V core voltage
- High signal-integrity flip-chip packaging available in standard or Pb-free package options

2.3 FPGA Configuration (Virtex-5)

The Virtex-5 FPGA is configured by loading application-specific configuration data - the bitstream - into internal memory. Because the Xilinx FPGA configuration memory is volatile, it must be configured each time it is powered-up. The bitstream is loaded into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes. The following configuration modes are supported:

- Slave SelectMAP (parallel) configuration mode (x8)
- Master Serial Peripheral Interface (SPI) Flash configuration mode
- JTAG/Boundary-Scan configuration mode

The configuration modes are explained in detail in Chapter 2, Configuration Interfaces of the UG191 - Virtex-5 FPGA Configuration User Guide. The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0]. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or VCC_CONFIG, see Figure 14. The mode pins should not be toggled during and after configuration. The configuration/mode pins can also be driven by the Marvell MV78200 CPU in Slave SelectMAP mode.

2.3.1 Configuration FPGA M[2..0] Select Resistors

The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0] configuration pins.

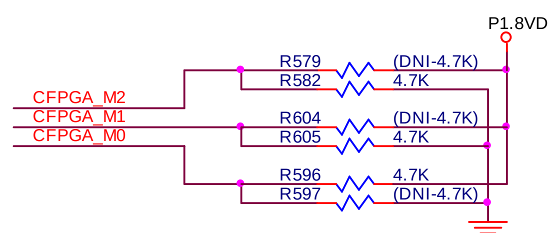


Figure 14 – Configuration FPGA M[2..0] Select Resistors (default Slave SelectMAP)

Select the configuration scheme by driving the Configuration FPGA M[2..0] pins either HIGH or LOW as shown in Table 11.

Table 11 – Configuration FPGA Configuration Schemes

Configuration Mode	M[2:0]	Configuration Resistors
Slave SelectMAP	110	R579, R604, R597 Installed
Master SPI	001	R582, R605, R579 Installed
JTAG	101	R579, R606, R596 Installed

2.3.2 SelectMAP via Marvell CPU

The Marvell MPP bus is connected to the SelectMAP interface on the Configuration FPGA. The SelectMAP configuration interface provides an 8-bit bidirectional data bus interface to the Virtex-5 configuration logic that can be used for both configuration and readback. CCLK is an input to the Configuration FPGA in Slave SelectMAP mode. Table 12 shows the MPP bus connection between the Marvell CPU and the Configuration FPGA.

Table 12 – SelectMAP Bus between Marvell 78200 CPU and Configuration FPGA

Signal Name	CPU	Configuration FPGA
D0 (MPP0)	U4-AA18	U17-AD19
D1 (MPP1)	U4-AA19	U17-AE19
D2 (MPP2)	U4-AB19	U17-AE17
D3 (MPP3)	U4-AC19	U17-AF16
D4 (MPP4)	U4-AD19	U17-AD20
D5 (MPP5)	U4-AE19	U17-AE21
D6 (MPP6)	U4-AF19	U17-AE16
D7 (MPP7)	U4-AD20	U17-AF15
CFPGA_M0 (MPP8)	U4-AF20	U17-AD21
CFPGA_M1 (MPP9)	U4-AA21	U17-AC22
CFPGA_M2 (MPP10)	U4-AB21	U17-AD22
CFPGA_BUSY (MPP11)	U4-AC21	U17-AD15
CFPGA_DONE (MPP16)	U4-AD22	U17-M15
CFPGA_INITn (MPP17)	U4-AE22	U17-N14
CFPGA_CCLK_18 (MPP18)	U4-AB23	U17-N15
CFPGA_RD/WRn (MPP19)	U4-AC23	U17-N23
CFPGA_CSn (MPP20)	U4-AD23	U17-N22
CFPGA_PROGn_CPU (MPP21)	U4-AE23	U17-M22

2.3.3 SPI Serial Flash

In SPI serial Flash mode, M[2:0] = 001., the Virtex-5 FPGA configures itself from an attached industry-standard SPI serial Flash PROM (M25P128). Voltage translators are used to interface the PROM to the Configuration Bank (VCCO – 1.8V). Although SPI is a standard four-wire interface, various available SPI Flash memories use different read commands and protocol. Besides M[2:0], FS[2:0] pins are sampled by the INIT_B rising edge to determine the type of read commands used by SPI Flash, see Figure 15.

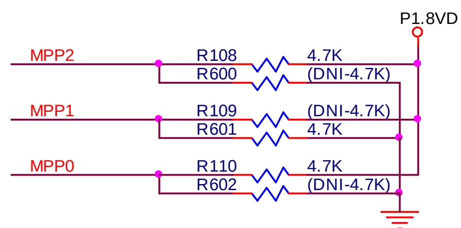


Figure 15 - SPI Variant Select Resistors

For Virtex-5 FPGA configurations, the default address always starts from 0. Table 13 shows the SPI related configuration pins, and the standard connection between the Configuration FPGA and the SPI Flash.

Table 13 – Connection between SPI Flash and the Configuration FPGA

Signal Name	SPI Flash	Configuration FPGA
SPI_FLASH_MOSI_18	U48.15	U17-AF14
SPI_FLASH_FCSn_18	U48.7	U17-AF14
CFPGA_CCLK_18	U48.16	U17-N15
CFPGA_D_IN_18	U48.8	U17-P15

2.3.4 JTAG

Virtex-5 devices support IEEE standards 1149.1 and 1532. IEEE 1532 is a standard for In-System Configuration (ISC), based on the IEEE 1149.1 standard. JTAG is an acronym for the Joint Test Action Group, the technical subcommittee initially responsible for developing the standard. This standard provides a means to ensure the board-level integrity of individual components and the interconnections between them. The IEEE 1149.1 Test Access Port and Boundary-Scan Architecture is commonly referred to as JTAG. JTAG connector (J12) used to download the configuration files to the Configuration FPGA, see Figure 16.

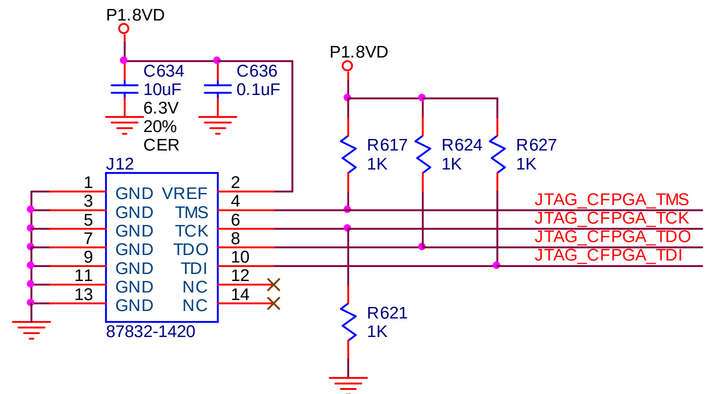


Figure 16 - Configuration FPGA JTAG Interface

Table 14 shows the connection between the JTAG header and the Configuration FPGA JTAG.

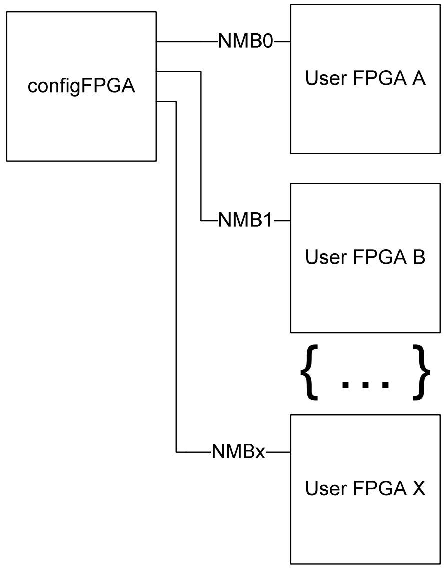
Table 14 – Connection between JTAG Header and Configuration FPGA

Signal Name	Configuration FPGA	Connector
JTAG_CFPGA_TCK	U17.AB5	J12.6
JTAG_CFPGA_TDI	U17.AC15	J12.10
JTAG_CFPGA_TDO_F	U17.AD14	J12.8
JTAG_CFPGA_TMS	U17.AC14	J12.4

2.4 Interconnect – Configuration FPGA to FPGA A/B

2.4.1 Not Main Bus (NMB)

A dedicated, point-to-point, high-speed (LVDS) “Not Main Bus” (NMB) bus is provided between the Configuration FPGA and FPGA A and FPGA B respectively.



NMB is a 10-bit bus (9-data + 1 source-synchronous clock) in each direction with a maximum operating speed of 1 Gbps per signal, for a total of 9 Gbps in each direction (full-duplex). See Figure 17 for the NMB between the Configuration FPGA and FPGA A.

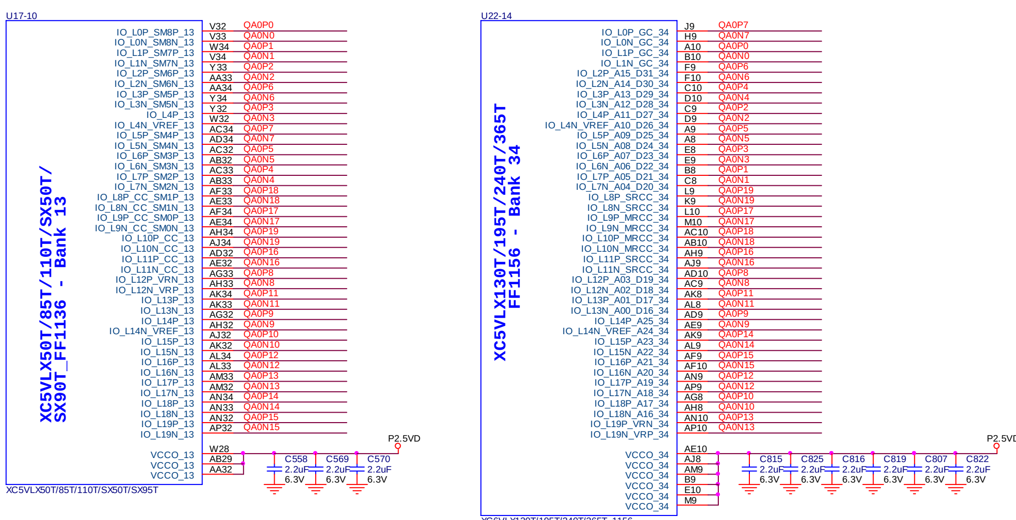


Figure 17 - Not Main Bus (NMB) to FPGA A

In Source Synchronous mode, QA0[P/N][18-19] can be used as the clock signal. Table 15 shows the connection between the Configuration FPGA and FPGA A.

Table 15 - Connections between the Configuration FPGA and FPGA A

Signal Name	Configuration FPGA	FPGA A
QA0N0	U17-V33	U22-B10
QA0N1	U17-V34	U22-C8
QA0N10	U17-AK32	U22-AH8
QA0N11	U17-AK33	U22-AL8
QA0N12	U17-AL33	U22-AP9
QA0N13	U17-AM32	U22-AP10
QA0N14	U17-AN33	U22-AL9
QA0N15	U17-AP32	U22-AF10
QA0N16	U17-AE32	U22-AJ9
QA0N17	U17-AE34	U22-M10
QA0N18	U17-AE33	U22-AB10
QA0N19	U17-AJ34	U22-K9
QA0N2	U17-AA33	U22-D9
QA0N3	U17-W32	U22-E9
QA0N4	U17-AB33	U22-D10
QA0N5	U17-AB32	U22-A8
QA0N6	U17-Y34	U22-F10
QA0N7	U17-AD34	U22-H9
QA0N8	U17-AH33	U22-AC9
QA0N9	U17-AH32	U22-AE9
QA0P0	U17-V32	U22-A10
QA0P1	U17-W34	U22-B8
QA0P10	U17-AJ32	U22-AG8
QA0P11	U17-AK34	U22-AK8
QA0P12	U17-AL34	U22-AN9
QA0P13	U17-AM33	U22-AN10
QA0P14	U17-AN34	U22-AK9
QA0P15	U17-AN32	U22-AF9
QA0P16	U17-AD32	U22-AH9
QA0P17	U17-AF34	U22-L10
QA0P18	U17-AF33	U22-AC10

Signal Name	Configuration FPGA	FPGA A
QA0P19	U17-AH34	U22-L9
QA0P2	U17-Y33	U22-C9
QA0P3	U17-Y32	U22-E8
QA0P4	U17-AC33	U22-C10
QA0P5	U17-AC32	U22-A9
QA0P6	U17-AA34	U22-F9
QA0P7	U17-AC34	U22-J9
QA0P8	U17-AG33	U22-AD10
QA0P9	U17-AG32	U22-AD9

Table 16 shows the connection between the Configuration FPGA and FPGA B.

Table 16 - Connections between the Configuration FPGA and FPGA B

Signal Name	Configuration FPGA	FPGA B
QB0N0	U17-T34	U24-AP9
QB0N1	U17-R34	U24-AL8
QB0N10	U17-D32	U24-B10
QB0N11	U17-D34	U24-D10
QB0N12	U17-A33	U24-D9
QB0N13	U17-H32	U24-AE9
QB0N14	U17-H33	U24-AL9
QB0N15	U17-J34	U24-F10
QB0N16	U17-N32	U24-K9
QB0N17	U17-U31	U24-AB10
QB0N18	U17-K34	U24-M10
QB0N19	U17-K32	U24-AJ9
QB0N2	U17-R32	U24-AH8
QB0N3	U17-N34	U24-AF10
QB0N4	U17-C33	U24-AP10
QB0N5	U17-M33	U24-AC9
QB0N6	U17-M32	U24-H9

Signal Name	Configuration FPGA	FPGA B
QB0N7	U17-E33	U24-E9
QB0N8	U17-F34	U24-A8
QB0N9	U17-E34	U24-C8
QB0P0	U17-U33	U24-AN9
QB0P1	U17-T33	U24-AK8
QB0P10	U17-C32	U24-A10
QB0P11	U17-C34	U24-C10
QB0P12	U17-B32	U24-C9
QB0P13	U17-G32	U24-AD9
QB0P14	U17-J32	U24-AK9
QB0P15	U17-H34	U24-F9
QB0P16	U17-P32	U24-L9
QB0P17	U17-U32	U24-AC10
QB0P18	U17-L34	U24-L10
QB0P19	U17-K33	U24-AH9

2.4.2 Fast Bus (Optional)

The unused IO Banks on the Configuration FPGA, labeled as Fast Bus (LVDS), is connected between the Configuration FPGA and FPGA A. This interface is available to the User, although the Dini Group has no specific purpose for this bus. Table 17 shows the connection between the Configuration FPGA and FPGA A.

Table 17 – Fast Bus connections between the Configuration FPGA and FPGA A

Signal Name	Configuration FPGA	FPGA A
QA1N0	U17-V24	U22-AA29
QA1N1	U17-V27	U22-AA31
QA1N10	U17-AH30	U22-AG32
QA1N11	U17-AG31	U22-AF31
QA1N12	U17-AE31	U22-AC28
QA1N13	U17-Y31	U22-AC27
QA1N14	U17-Y29	U22-AA33
QA1N15	U17-AC30	U22-AC32

Signal Name	Configuration FPGA	FPGA A
QA1N16	U17-AC29	U22-AC30
QA1N17	U17-AA31	U22-AF34
QA1N18	U17-AA30	U22-AF33
QA1N19	U17-W26	U22-AC29
QA1N2	U17-W27	U22-AB31
QA1N3	U17-AD29	U22-AB26
QA1N4	U17-W30	U22-Y26
QA1N5	U17-W25	U22-AC25
QA1N6	U17-V29	U22-AB33
QA1N7	U17-AF30	U22-AC34
QA1N8	U17-AG30	U22-AE32
QA1N9	U17-AK31	U22-AD31
QA1P0	U17-W24	U22-AA28
QA1P1	U17-V28	U22-AA30
QA1P10	U17-AJ30	U22-AG33
QA1P11	U17-AF31	U22-AG31
QA1P12	U17-AD31	U22-AB28
QA1P13	U17-W31	U22-AB27
QA1P14	U17-Y28	U22-AA34
QA1P15	U17-AB30	U22-AB32
QA1P16	U17-AD30	U22-AD30
QA1P17	U17-AB31	U22-AE34
QA1P18	U17-AA29	U22-AE33
QA1P19	U17-Y26	U22-AD29
QA1P2	U17-Y27	U22-AB30
QA1P3	U17-AE29	U22-AA26
QA1P4	U17-V30	U22-AA25
QA1P5	U17-V25	U22-AB25
QA1P6	U17-W29	U22-AC33
QA1P7	U17-AF29	U22-AD34
QA1P8	U17-AH29	U22-AD32

Signal Name	Configuration FPGA	FPGA A
QA1P9	U17-AJ31	U22-AE31
QA2N0	U17-Y7	U22-L26
QA2N1	U17-W9	U22-J27
QA2N10	U17-AK6	U22-F34
QA2N11	U17-AJ6	U22-G30
QA2N12	U17-AG7	U22-H32
QA2N13	U17-AE6	U22-H33
QA2N14	U17-AD7	U22-H30
QA2N15	U17-Y6	U22-J29
QA2N16	U17-AF6	U22-C34
QA2N17	U17-AF5	U22-E31
QA2N18	U17-V7	U22-K27
QA2N19	U17-Y9	U22-G33
QA2N2	U17-V9	U22-J32
QA2N3	U17-W11	U22-J34
QA2N4	U17-U8	U22-K29
QA2N5	U17-AB5	U22-B32
QA2N6	U17-AB7	U22-B34
QA2N7	U17-AC5	U22-B33
QA2N8	U17-AD5	U22-D32
QA2N9	U17-AG6	U22-E33
QA2P0	U17-AA6	U22-L25
QA2P1	U17-W10	U22-J26
QA2P10	U17-AK7	U22-E34
QA2P11	U17-AJ7	U22-F30
QA2P12	U17-AH7	U22-G32
QA2P13	U17-AD6	U22-H34
QA2P14	U17-AC7	U22-G31
QA2P15	U17-W6	U22-K28
QA2P16	U17-AE7	U22-D34
QA2P17	U17-AG5	U22-F31

Signal Name	Configuration FPGA	FPGA A
QA2P18	U17-W7	U22-K26
QA2P19	U17-Y8	U22-F33
QA2P2	U17-V10	U22-J31
QA2P3	U17-Y11	U22-K33
QA2P4	U17-V8	U22-J30
QA2P5	U17-AA5	U22-C32
QA2P6	U17-AB6	U22-C33
QA2P7	U17-AC4	U22-A33
QA2P8	U17-AD4	U22-D31
QA2P9	U17-AH5	U22-E32
QA3N0	U17-AC24	U22-T29
QA3N1	U17-AB26	U22-T31
QA3N10	U17-AG26	U22-Y31
QA3N11	U17-AE26	U22-Y27
QA3N12	U17-AD27	U22-V25
QA3N13	U17-AJ27	U22-R34
QA3N14	U17-AK27	U22-T34
QA3N15	U17-AJ29	U22-U27
QA3N16	U17-AJ26	U22-U30
QA3N17	U17-AA28	U22-W34
QA3N18	U17-AA26	U22-W30
QA3N19	U17-AA24	U22-V27
QA3N2	U17-AC27	U22-T25
QA3N3	U17-AD25	U22-V29
QA3N4	U17-AE24	U22-W26
QA3N5	U17-AF28	U22-U32
QA3N6	U17-AG25	U22-W32
QA3N7	U17-AH25	U22-V33
QA3N8	U17-AF26	U22-Y29
QA3N9	U17-AH28	U22-Y34
QA3P0	U17-AC25	U22-T28

Signal Name	Configuration FPGA	FPGA A
QA3P1	U17-AB25	U22-T30
QA3P10	U17-AG27	U22-Y32
QA3P11	U17-AE27	U22-Y28
QA3P12	U17-AC28	U22-W25
QA3P13	U17-AK26	U22-R33
QA3P14	U17-AK28	U22-T33
QA3P15	U17-AK29	U22-U26
QA3P16	U17-AH27	U22-U31
QA3P17	U17-AB28	U22-V34
QA3P18	U17-AA25	U22-V30
QA3P19	U17-Y24	U22-V28
QA3P2	U17-AB27	U22-U25
QA3P3	U17-AD26	U22-U28
QA3P4	U17-AD24	U22-W27
QA3P5	U17-AE28	U22-U33
QA3P6	U17-AF24	U22-W31
QA3P7	U17-AJ25	U22-V32
QA3P8	U17-AF25	U22-W29
QA3P9	U17-AG28	U22-Y33
QA4N0	U17-AC9	U22-R29
QA4N1	U17-AA10	U22-R27
QA4N10	U17-AJ10	U22-M32
QA4N11	U17-AH8	U22-M28
QA4N12	U17-AF10	U22-M25
QA4N13	U17-AD11	U22-T26
QA4N14	U17-AL10	U22-R32
QA4N15	U17-AJ11	U22-P30
QA4N16	U17-AE11	U22-P32
QA4N17	U17-AE9	U22-M33
QA4N18	U17-AD9	U22-L30
QA4N19	U17-AB8	U22-N29

Signal Name	Configuration FPGA	FPGA A
QA4N2	U17-AA9	U22-P26
QA4N3	U17-AP14	U22-P27
QA4N4	U17-AG11	U22-M27
QA4N5	U17-AM13	U22-N30
QA4N6	U17-AN12	U22-P34
QA4N7	U17-AM11	U22-L31
QA4N8	U17-AH10	U22-L34
QA4N9	U17-AK9	U22-K31
QA4P0	U17-AC10	U22-P29
QA4P1	U17-AB10	U22-R28
QA4P10	U17-AJ9	U22-L33
QA4P11	U17-AG8	U22-L28
QA4P12	U17-AF9	U22-N25
QA4P13	U17-AD10	U22-R26
QA4P14	U17-AL11	U22-R31
QA4P15	U17-AK11	U22-P31
QA4P16	U17-AF11	U22-N32
QA4P17	U17-AF8	U22-N33
QA4P18	U17-AE8	U22-L29
QA4P19	U17-AC8	U22-N28
QA4P2	U17-AA8	U22-P25
QA4P3	U17-AN14	U22-N27
QA4P4	U17-AG10	U22-M26
QA4P5	U17-AN13	U22-M30
QA4P6	U17-AP12	U22-N34
QA4P7	U17-AM12	U22-M31
QA4P8	U17-AH9	U22-K34
QA5N0	U17-P24	U22-AD27
QA5N1	U17-M26	U22-AE29
QA5N10	U17-K26	U22-AJ30
QA5N11	U17-P27	U22-AM32

Signal Name	Configuration FPGA	FPGA A
QA5N12	U17-J26	U22-AP33
QA5N13	U17-H27	U22-AH32
QA5N14	U17-F28	U22-AH34
QA5N15	U17-G28	U22-AF29
QA5N16	U17-E27	U22-AN34
QA5N17	U17-G26	U22-AG30
QA5N18	U17-L24	U22-AG28
QA5N19	U17-J25	U22-AE26
QA5N2	U17-L26	U22-AD26
QA5N3	U17-N25	U22-AH30
QA5N4	U17-T24	U22-AM31
QA5N5	U17-F26	U22-AK34
QA5N6	U17-L28	U22-AL33
QA5N7	U17-M27	U22-AJ32
QA5N8	U17-N28	U22-AK31
QA5N9	U17-H24	U22-AK32
QA5P0	U17-N24	U22-AE27
QA5P1	U17-M25	U22-AE28
QA5P10	U17-K27	U22-AJ29
QA5P11	U17-P26	U22-AN32
QA5P12	U17-J27	U22-AP32
QA5P13	U17-G27	U22-AH33
QA5P14	U17-E28	U22-AJ34
QA5P15	U17-H28	U22-AF28
QA5P16	U17-E26	U22-AN33
QA5P17	U17-G25	U22-AF30
QA5P18	U17-K24	U22-AG27
QA5P19	U17-J24	U22-AF26
QA5P2	U17-L25	U22-AD25
QA5P3	U17-P25	U22-AH29
QA5P4	U17-R24	U22-AL30

Signal Name	Configuration FPGA	FPGA A
QA5P5	U17-F25	U22-AL34
QA5P6	U17-K28	U22-AM33
QA5P7	U17-N27	U22-AJ31
QA5P8	U17-M28	U22-AL31
QA5P9	U17-H25	U22-AK33

2.4.3 High-Speed Interconnect (GTP) to FPGA A/B

Two high-speed serial channels are provided between the Configuration FPGA and FPGA A/B. This could be used for pin multiplexing, 10x pin per LVDS pair. The GTP transceiver is highly configurable and tightly integrated with the programmable logic resources of the FPGA. It provides the following features to support a wide variety of applications:

- Current Mode Logic (CML) serial drivers/buffers with configurable termination, voltage swing, and coupling
- Programmable TX pre-emphasis and RX equalization for optimized signal integrity
- Line rates from 100 Mb/s to 3.75 Gb/s, with optional 5x digital oversampling required for rates between 100 Mb/s and 500 Mb/s
- Optional built-in PCS features, such as 8B/10B encoding, comma alignment, channel bonding, and clock correction
- Fixed latency modes for minimized, deterministic datapath latency
- Beacon signaling for PCI Express designs and Out-of-Band signaling including
- COM signal support for SATA designs

The Xilinx CORE Generator tool includes a Wizard to automatically configure GTP transceivers to support one of various protocols or perform custom configuration (see "*UG-198 – Virtex-5 RocketIO GTX Transceiver User Guide*").

GTP transceivers are placed as dual transceiver GTP_DUAL tiles in Virtex-5 LXT and SXT Platform devices. This configuration allows two transceivers to share a single PLL with the TX and RX functions of both, reducing size and power consumption.

Table 18 shows the connection between the Configuration FPGA and FPGA A/B. In-line AC-Coupling capacitors are provided for DC isolation from the Transmitter.

Table 18 – High-Speed Serial connection between the Configuration FPGA and FPGA A/B

Signal Name	Configuration FPGA	FPGA A/B
HS_CF_A_TXP0	U17-AK2	U22-G3
HS_CF_A_TXN0	U17-AL2	U22-G4
HS_CF_A_RXP0	U17-AL1	U22-D1
HS_CF_A_RXN0	U17-AM1	U22-D2
HS_CF_A_TXP1	U17-AN4	U22-E3
HS_CF_A_TXN1	U17-AN3	U22-E4
HS_CF_A_RXP1	U17-AP3	U22-C3
HS_CF_A_RXN1	U17-AP2	U22-C4
HS_CF_B_TXP0	U17-AD2	U24-AP5
HS_CF_B_TXN0	U17-AE2	U24-AP6
HS_CF_B_RXP0	U17-AE1	U24-AP1
HS_CF_B_RXN0	U17-AF1	U24-AP2
HS_CF_B_TXP1	U17-AJ2	U24-AM5
HS_CF_B_TXN1	U17-AH2	U24-AM6
HS_CF_B_RXP1	U17-AH1	U24-AN3
HS_CF_B_RXN1	U17-AG1	U24-AN4

3 FPGA A/B (Virtex-6)

3.1 Overview

The Virtex-6 family provides the newest, most advanced features in the FPGA market. Virtex-6 FPGAs are the programmable silicon foundation for Targeted Design Platforms that deliver integrated software and hardware components to enable designers to focus on innovation as soon as their development cycle begins. Using the third-generation ASMBL (Advanced Silicon Modular Block) column based architecture, the Virtex-6 family contains multiple distinct sub-families. This overview covers the devices in the LXT, SXT, and HXT sub-families. Each sub-family contains a different ratio of features to most efficiently address the needs of a wide variety of advanced logic designs. In addition to the high-performance logic fabric, Virtex-6 FPGAs contain many built-in system-level blocks. These features allow logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 40 nm state-of-the art copper process technology, Virtex-6 FPGAs are a programmable alternative to custom ASIC technology. Virtex-6 FPGAs offer the best solution for addressing the needs of high-performance logic designers, high-performance DSP designers, and high-performance embedded systems designers with unprecedented logic, DSP, connectivity, and soft microprocessor capabilities. For more information, please reference the Xilinx Virtex-6 documentation.

3.2 Summary of Virtex-6 FPGA Features

- Three sub-families:
    - Virtex-6 LXT FPGAs: High-performance logic with advanced serial connectivity
    - Virtex-6 SXT FPGAs: Highest signal processing capability with advanced serial connectivity
    - Virtex-6 HXT FPGAs: Highest bandwidth serial connectivity
- Compatibility across sub-families
    - LXT and SXT devices are footprint compatible in the same package
- Advanced, high-performance FPGA Logic
    - Real 6-input look-up table (LUT) technology
    - Dual LUT5 (5-input LUT) option
    - LUT/dual flip-flop pair for applications requiring rich register mix
    - Improved routing efficiency
    - 64-bit (or 32 x 2-bit) distributed LUT RAM option
    - SRL32/dual SRL16 with registered outputs option
- Powerful mixed-mode clock managers (MMCM)
    - MMCM blocks provide zero-delay buffering, frequency synthesis, clock-phase shifting, input-jitter filtering, and phase-matched clock division
- 36-Kb block RAM/FIFOs
    - Dual-port RAM blocks
    - Programmable
    - Dual-port widths up to 36 bits
    - Simple dual-port widths up to 72 bits
    - Enhanced programmable FIFO logic
    - Built-in optional error-correction circuitry
    - Optionally use each block as two independent 18 Kb blocks
- High-performance parallel SelectIO technology
    - 1.2 to 2.5V I/O operation

- Source-synchronous interfacing using
- ChipSync™ technology
- Digitally controlled impedance (DCI) active termination
- Flexible fine-grained I/O banking
- High-speed memory interface support with integrated write-leveling capability

- Advanced DSP48E1 slices
  - 25 x 18, two's complement multiplier/accumulator
  - Optional pipelining
  - New optional pre-adder to assist filtering applications
  - Optional bitwise logic functionality
  - Dedicated cascade connections
- Flexible configuration options
  - SPI and Parallel Flash interface
  - Multi-bitstream support with dedicated fallback reconfiguration logic
  - Automatic bus width detection
- System Monitor capability on all devices
  - On-chip/off-chip thermal and supply voltage monitoring
  - JTAG access to all monitored quantities
- Integrated interface blocks for PCI Express® designs
  - Designed to the PCI Express Base Specification 2.0
  - Gen1 (2.5 Gb/s) and Gen2 (5 Gb/s) support with GTX transceivers
  - Endpoint and Root Port capable
  - x1, x2, x4, or x8 lane support per block
- GTX transceivers: 150 Mb/s to 6.5 Gb/s
- GTH transceivers: 2.488 Gb/s to beyond 11 Gb/s
- Integrated 10/100/1000 Mb/s Ethernet MAC block
  - Supports 1000BASE-X PCS/PMA and SGMII using GTX transceivers
  - Supports MII, GMII, and RGMII using SelectIO technology resources

  - o 2500Mb/s support available
- 40 nm copper CMOS process technology
- 1.0V core voltage (-1, -2, -3 speed grades only)
- Lower-power 0.9V core voltage option (-1L speed grade only)
- High signal-integrity flip-chip packaging available in standard or Pb-free package options

3.3 FPGA Configuration (Virtex-6)

Virtex-6 FPGAs are configured by loading application-specific configuration data - the bitstream - into internal memory. Because the Xilinx FPGA configuration memory is volatile, it must be configured each time it is powered-up. The bitstream is loaded into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes. The following configuration modes are supported:

- Slave SelectMAP (parallel) configuration mode (x8)
- JTAG/Boundary-Scan configuration mode

The configuration modes are explained in detail in Chapter 2, Configuration Interfaces of the UG360 - Virtex-6 FPGA Configuration User Guide. The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0]. The M2, M1, and M0 mode pins should be set at a constant DC voltage level, either through pull-up or pull-down resistors, or tied directly to ground or VCC_CONFIG, see Figure 18. The mode pins should not be toggled during and after configuration. The mode pins can also be driven by the CPU in Slave SelectMAP mode. The mode pins should not be toggled during and after configuration.

In Slave SelectMAP mode, FPGA A and FPGA B are independently configured from the Configuration FPGA. The mode pins can also be driven by the Configuration FPGA (U17) in Slave SelectMAP mode, thus two sets of configuration mode select resistor exists, see Figure 18.

3.3.1 FPGA A/B M[2..0] Select Resistors

The specific configuration mode is selected by setting the appropriate level on the dedicated Mode input pins M[2:0] configuration pins.

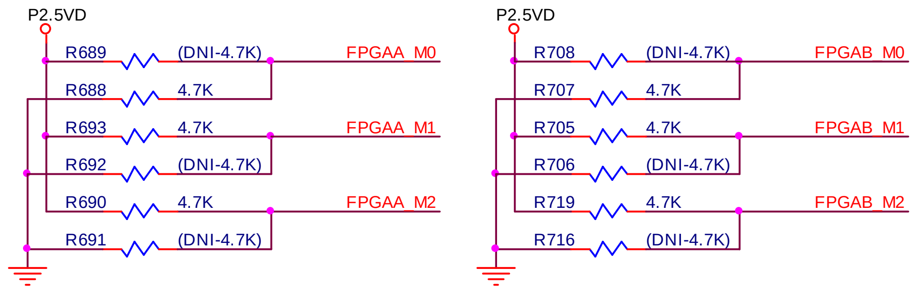


Figure 18 - FPGA A/B M[2..0] Select Resistors (default Slave SelectMAP)

Select the configuration scheme by driving the Configuration FPGA M[2..0] pins either HIGH or LOW as shown in Table 19.

Table 19 – FPGA A/B Configuration Schemes

Configuration Mode	M[2:0]	Configuration Resistors
FPGA A		
Slave SelectMAP	110	R690, R693, R688 Installed
JTAG	101	R690, R692, R689 Installed
FPGA B		
Slave SelectMAP	110	R719, R705, R707 Installed
JTAG	101	R719, R706, R708 Installed

3.3.2 SelectMAP via Configuration FPGA

The Configuration FPGA (U17) is connected to the SelectMAP interface on FPGA A (U22) and FPGA B (U24) with a dedicated 8-bit bidirectional data bus. This allows for faster data transfer and independent FPGA configuration during configuration or readback. CCLK is an input in Slave SelectMAP mode. Table 20 shows the SelectMAP bus connection between the Configuration FPGA and FPGA A/B.

Table 20 – SelectMAP Bus between Configuration FPGA and FPGA A/B

Signal Name	Configuration FPGA	FPGA A/B
FPGAA_D0	U17-L4	U22-AF24
FPGAA_D1	U17-P5	U22-AF25
FPGAA_D2	U17-N5	U22-W24
FPGAA_D3	U17-L6	U22-V24
FPGAA_D4	U17-M7	U22-H24
FPGAA_D5	U17-N7	U22-H25
FPGAA_D6	U17-N8	U22-P24

Signal Name	Configuration FPGA	FPGA A/B
FPGAA_D7	U17-M5	U22-R24
FPGAA_CCLK	U17-M6	U22-K8
FPGAA_PROGN	U17-L5	U22-L8
FPGAA_BUSY	U17-P7	U22-AA8
FPGAA_RD/WRN	U17-P6	U22-G8
FPGAA_INITN	U17-K7	U22-P8
FPGAA_CSN	U17-K6	U22-F8
FPGAA_DONE	U17-R6	U22-R8
FPGAA_M0	U17-J5	U22-U8
FPGAA_M1	U17-J6	U22-W8
FPGAA_M2	U17-T6	U22-V8
FPGAB_D0	U17-L29	U24-AF24
FPGAB_D1	U17-E31	U24-AF25
FPGAB_D2	U17-F31	U24-W24
FPGAB_D3	U17-J29	U24-V24
FPGAB_D4	U17-H29	U24-H24
FPGAB_D5	U17-F30	U24-H25
FPGAB_D6	U17-G30	U24-P24
FPGAB_D7	U17-F29	U24-R24
FPGAB_CCLK	U17-E29	U24-K8
FPGAB_PROGN	U17-K29	U24-L8
FPGAB_BUSY	U17-H30	U24-AA8
FPGAB_RD/WRN	U17-G31	U24-G8
FPGAB_INITN	U17-J30	U24-P8
FPGAB_CSN	U17-J31	U24-F8
FPGAB_DONE	U17-L30	U24-R8
FPGAB_M0	U17-P29	U24-U8
FPGAB_M1	U17-N29	U24-W8
FPGAB_M2	U17-M30	U24-V8

3.3.3 JTAG

Virtex-6 devices support IEEE standards 1149.1 and 1532. IEEE 1532 is a standard for In-System Configuration (ISC), based on the IEEE 1149.1 standard. JTAG is an acronym for the Joint Test Action Group, the technical subcommittee initially

responsible for developing the standard. This standard provides a means to ensure the board-level integrity of individual components and the interconnections between them. The IEEE 1149.1 Test Access Port and Boundary-Scan Architecture is commonly referred to as JTAG. JTAG connector (J13) is used to download the configuration files to the Configuration FPGA, see Figure 19.

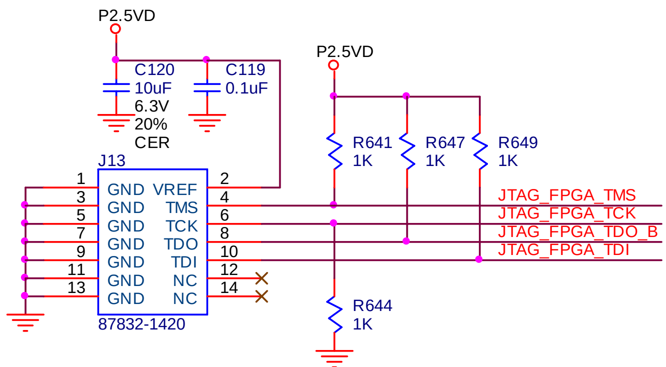


Figure 19 – FPGA A/B JTAG Interface

Table 21 shows the connection between the JTAG header and FPGA A/B.

Table 21 – Connection between JTAG Header and FPGA A/B

Signal Name	Connector	FPGA A/B
JTAG_FPGA_TCK	J13.6	U17-U26, U22-AE8, U24-AE8
JTAG_FPGA_TDI	J13.10	U18-T25, U22-AD8
JTAG_FPGA_TDO_B	J13.8	U18-U25, U24-AC8
JTAG_FPGA_TMS	J13.4	U22-AF8, U24-AF8

3.4 DDR3 Memory (SODIMM)

The DN-DualV6-PCIe-4 supports two 64-bit, 204 pin SODIMM modules connected to the Virtex-6 FPGA A and B, allowing addressing for up to 4GB DDR3 SDRAM (PC3-8500) modules. The following transfer speed can be expected:

- Speed Grade -3 1066Mb/s
- Speed Grade -2 1066Mb/s
- Speed Grade -1 800Mb/s

The interface is connected to IO Banks on the Virtex-6 FPGAs and uses a 1.5V switching power supply for V_{DD} and V_{CCIO}. V_{TT} and V_{REF} are powered from a separate linear power supply set at 0.75V DDR3 SDRAM modules are available from Micron,

example part number for a 4GB (512Meg x 64) 204-pin SODIMM SDRAM module is: MT16JSF51264HZ-1G1.

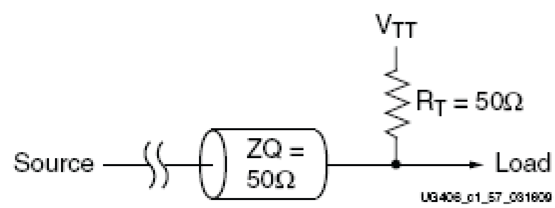
3.4.1 DDR3 SDRAM Memory Interface Solution

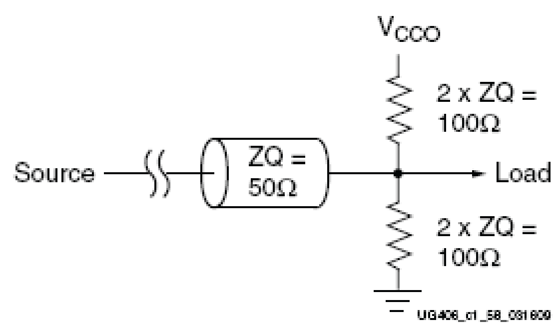
The Virtex-6 FPGA memory interface solutions core is a pre-engineered controller and physical layer (PHY) for interfacing Virtex-6 FPGA user designs to DDR2 and DDR3 SDRAM devices. The Memory Interface Generator (MIG) is a self-explanatory wizard tool that can be invoked under the CORE Generator software. This section is intended to help in understanding the various steps involved in using the MIG tool. Xilinx published a memory application note; please refer to *UG-406 - Virtex-6 FPGA Memory Interface Solutions, User Guide*.

3.4.2 DDR3 Termination

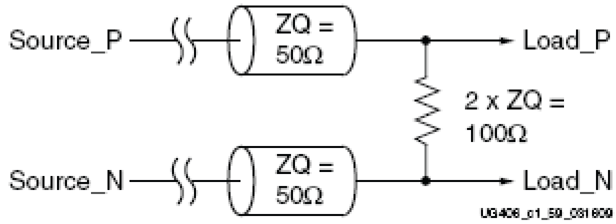
These rules apply to termination for DDR3 SDRAM:

- Unidirectional signals are to be terminated with the memory device's internal termination or a pull-up of 50Ω to VTT at the load. A split 100Ω termination to VCCO and a 100Ω termination to GND can be used, but takes more power. For bidirectional signals, the termination is needed at both ends of the signal (DCI/ODT or external termination).





- Differential signals should be terminated with the memory device's internal termination or a 100Ω differential termination at the load. For bidirectional signals, termination is needed at both ends of the signal (DCI/ODT or external termination).



- All termination must be placed as close to the load as possible. The termination can be placed before or after the load provided that the termination is placed within a small distance of the load pin. The allowable distance can be determined by simulation.
- DCI can be used at the FPGA as long as the DCI rules such as VRN/VRP are followed.
- The RESET and CKE signals are not terminated. These signals should be pulled down during memory initialization with a 4.7 kΩ resistor connected to GND.
- ODT, which terminates a signal at the memory, and DCI, which terminates a signal at the FPGA, are required. The MIG tool should be used to specify the configuration of the memory system for setting the mode register properly. Refer to Micron technical note TN-47-01 for additional details on ODT.
- ODT applies to the DQ, DQS, and DM signals only. If ODT is used, the mode register must be set appropriately to enable ODT at the memory.

3.4.3 V_{DD} Switching Power Supply (P_DIMM_x)

The Texas Instruments PTH12050 POLA DC-DC Converter is used to create the V_{DD} supply for the DDR3 SDRAM SODIMM, set to 1.5V @ 6A, see Figure 20. A jumper (JP2) allows the user to change the voltage to the SODIMM and the FPGA VCCO, see table (default jumper 1-3, 1.5V).

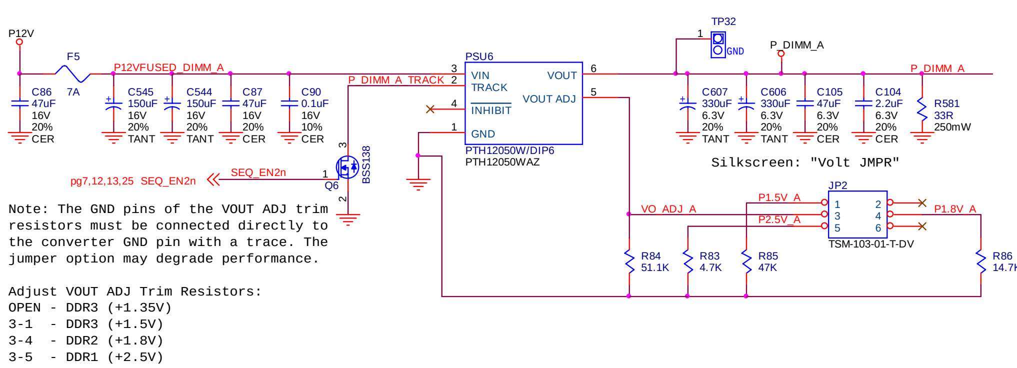


Figure 20 - VDD Switching Power Supply (P_DIMM_A)

3.4.4 VTT Linear Power Supply (P0.75V_VTT_x)

The Texas Instruments TPS51200 is a sink/source double data rate (DDR) termination regulator for termination of DDR3 SDRAM SODIMMs, see Figure 21.

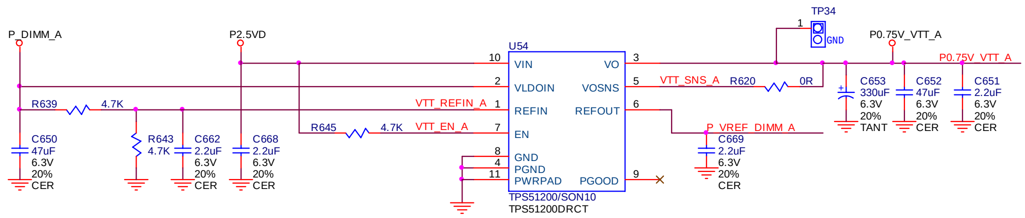


Figure 21 - VTT Linear Power Supply (P0.75V_VTT_A)

3.4.5 Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC Standard JC-45, "Appendix X: Serial Presence-Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. User-specific information can be written into the remaining 128 bytes of storage. READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[1:0], which provide four unique DIMM/EEPROM addresses. Write protect (WP) is connected to Vss internal to the Temp Sensor/EEPROM, permanently disabling hardware write protection. Please note that VDDSPD is connected to P3.3VD.

Table 22 - Serial Presence-Detect EEPROM Connections

Signal Name	FPGA	DDR3 SODIMM
SODIMM A (J14) – FPGA A (U22)		
DIMMA_SA0	U22-AM25	J14.197 pull-down with 4.7K (R614)
DIMMA_SA1	U22-AL25	J14.201 pull-down with 4.7K (R611)
DIMMA_SCL	U22-AD24	J14.202 pull-up 4.7K (R610)
DIMMA_SDA	U22-AE24	J14.195 pull-up 4.7K (R613)
SODIMM B (J21) – FPGA B (U24)		
DIMMB_SA0	U22-K13	J21.197 pull-down with 4.7K (R726)
DIMMB_SA1	U22-K12	J21.201 pull-down with 4.7K (R724)
DIMMB_SCL	U24-AE24	J21.202 pull-up 4.7K (R723)

DIMMB_SDA	U24-AD24	J21.200 pull-up 4.7K (R722)

3.4.6 Clocking Connections between FPGA A/B and DDR3 SDRAM SODIMMs

The clocking connections between the FPGA A/B and the DDR3 SDRAM SODIMMs are shown in Table 23.

Table 23 – Clocking Connections between FPGA A/B and the DDR3 SDRAM SODIMMs

Signal Name	FPGA	DDR3 SODIMM
SODIMM A (J14) – FPGA A (U22)		
DIMMA_CK0P	U22-AP11	J14-101
DIMMA_CK0N	U22-AP12	J14-103
DIMMA_CK1N	U22-AH24	J14-104
DIMMA_CK1P	U22-AH22	J14-102
SODIMM B (J21) – FPGA B (U24)		
DIMMB_CK0P	U24-D24	J21-101
DIMMB_CK0N	U24-E24	J21-103
DIMMB_CK1N	U24-J14	J21-104
DIMMB_CK1P	U24-K14	J21-102

3.4.7 SODIMM connections to the FPGA A/B

Table 24 shows the SODIMM connector pinouts and the connection to FPGA A/B.

Table 24 - Connections between the SODIMMs and FPGA A/B

Signal Name	SODIMM	FPGA
SODIMM A (J14) – FPGA A (U22)		
DIMMA_A0	J14-98	U22-AF18
DIMMA_A1	J14-97	U22-AE19
DIMMA_A10	J14-107	U22-AP22
DIMMA_A11	J14-84	U22-AH13
DIMMA_A12	J14-83	U22-AC17
DIMMA_A13	J14-119	U22-AP25
DIMMA_A14	J14-80	U22-AM13
DIMMA_A15	J14-78	U22-AN13
DIMMA_A2	J14-96	U22-AE18
DIMMA_A3	J14-95	U22-AP21

Signal Name	SODIMM	FPGA
DIMMA_A4	J14-92	U22-AM16
DIMMA_A5	J14-91	U22-AK16
DIMMA_A6	J14-90	U22-AM17
DIMMA_A7	J14-86	U22-AH14
DIMMA_A8	J14-89	U22-AL16
DIMMA_A9	J14-85	U22-AD16
DIMMA_BA0	J14-109	U22-AN23
DIMMA_BA1	J14-108	U22-AM22
DIMMA_BA2	J14-79	U22-AN14
DIMMA_CASN	J14-115	U22-AJ25
DIMMA_CK_FBN	U22-AD15	U22-AE17
DIMMA_CK_FBP	U22-AC15	U22-AD17
DIMMA_CK0N	J14-103	U22-AP12
DIMMA_CK0P	J14-101	U22-AP11
DIMMA_CK1N	J14-104	U22-AH24
DIMMA_CK1P	J14-102	U22-AH23
DIMMA_CKE0	J14-73	U22-AE14
DIMMA_CKE1	J14-74	U22-AH10
DIMMA_DM0	J14-11	U22-AF11
DIMMA_DM1	J14-28	U22-AK13
DIMMA_DM2	J14-46	U22-AG16
DIMMA_DM3	J14-63	U22-AJ19
DIMMA_DM4	J14-136	U22-AK22
DIMMA_DM5	J14-153	U22-AC19
DIMMA_DM6	J14-170	U22-AL29
DIMMA_DM7	J14-187	U22-AJ24
DIMMA_DQ0	J14-5	U22-AJ11
DIMMA_DQ1	J14-7	U22-AK11
DIMMA_DQ10	J14-33	U22-AM12
DIMMA_DQ11	J14-35	U22-AN12
DIMMA_DQ12	J14-22	U22-AM10
DIMMA_DQ13	J14-24	U22-AL10

Signal Name	SODIMM	FPGA
DIMMA_DQ14	J14-34	U22-AE13
DIMMA_DQ15	J14-36	U22-AE12
DIMMA_DQ16	J14-39	U22-AL15
DIMMA_DQ17	J14-41	U22-AL14
DIMMA_DQ18	J14-51	U22-AJ15
DIMMA_DQ19	J14-53	U22-AH15
DIMMA_DQ2	J14-15	U22-AL11
DIMMA_DQ20	J14-40	U22-AG15
DIMMA_DQ21	J14-42	U22-AF15
DIMMA_DQ22	J14-50	U22-AK14
DIMMA_DQ23	J14-52	U22-AJ14
DIMMA_DQ24	J14-57	U22-AP16
DIMMA_DQ25	J14-59	U22-AP15
DIMMA_DQ26	J14-67	U22-AN15
DIMMA_DQ27	J14-69	U22-AM15
DIMMA_DQ28	J14-56	U22-AJ17
DIMMA_DQ29	J14-58	U22-AJ16
DIMMA_DQ3	J14-17	U22-AM11
DIMMA_DQ30	J14-68	U22-AN17
DIMMA_DQ31	J14-70	U22-AP17
DIMMA_DQ32	J14-129	U22-AM18
DIMMA_DQ33	J14-131	U22-AL18
DIMMA_DQ34	J14-141	U22-AE21
DIMMA_DQ35	J14-143	U22-AD21
DIMMA_DQ36	J14-130	U22-AP19
DIMMA_DQ37	J14-132	U22-AN18
DIMMA_DQ38	J14-140	U22-AG22
DIMMA_DQ39	J14-142	U22-AH22
DIMMA_DQ4	J14-4	U22-AD14
DIMMA_DQ40	J14-147	U22-AN19
DIMMA_DQ41	J14-149	U22-AN20
DIMMA_DQ42	J14-157	U22-AM21

Signal Name	SODIMM	FPGA
DIMMA_DQ43	J14-159	U22-AL21
DIMMA_DQ44	J14-146	U22-AC20
DIMMA_DQ45	J14-148	U22-AD20
DIMMA_DQ46	J14-158	U22-AM20
DIMMA_DQ47	J14-160	U22-AL20
DIMMA_DQ48	J14-163	U22-AH27
DIMMA_DQ49	J14-165	U22-AH28
DIMMA_DQ5	J14-6	U22-AC14
DIMMA_DQ50	J14-175	U22-AN30
DIMMA_DQ51	J14-177	U22-AM30
DIMMA_DQ52	J14-164	U22-AG25
DIMMA_DQ53	J14-166	U22-AG26
DIMMA_DQ54	J14-174	U22-AP30
DIMMA_DQ55	J14-176	U22-AP31
DIMMA_DQ56	J14-181	U22-AN29
DIMMA_DQ57	J14-183	U22-AP29
DIMMA_DQ58	J14-191	U22-AL28
DIMMA_DQ59	J14-193	U22-AK28
DIMMA_DQ6	J14-16	U22-AK12
DIMMA_DQ60	J14-180	U22-AL26
DIMMA_DQ61	J14-182	U22-AM26
DIMMA_DQ62	J14-192	U22-AN28
DIMMA_DQ63	J14-194	U22-AM28
DIMMA_DQ7	J14-18	U22-AJ12
DIMMA_DQ8	J14-21	U22-AG11
DIMMA_DQ9	J14-23	U22-AG10
DIMMA_DQS0N	J14-10	U22-AD11
DIMMA_DQS0P	J14-12	U22-AD12
DIMMA_DQS1N	J14-27	U22-AH12
DIMMA_DQS1P	J14-29	U22-AG12
DIMMA_DQS2N	J14-45	U22-AG17
DIMMA_DQS2P	J14-47	U22-AH17

Signal Name	SODIMM	FPGA
DIMMA_DQS3N	J14-62	U22-AK17
DIMMA_DQS3P	J14-64	U22-AK18
DIMMA_DQS4N	J14-135	U22-AF21
DIMMA_DQS4P	J14-137	U22-AF20
DIMMA_DQS5N	J14-152	U22-AJ21
DIMMA_DQS5P	J14-154	U22-AK21
DIMMA_DQS6N	J14-169	U22-AJ27
DIMMA_DQS6P	J14-171	U22-AK27
DIMMA_DQS7N	J14-186	U22-AP26
DIMMA_DQS7P	J14-188	U22-AP27
DIMMA_EVENTN	J14-198	U22-AN25
DIMMA_NC0	J14-77	U22-AP14
DIMMA_NC2	J14-122	U22-AG20
DIMMA_NC3	J14-125	U22-AG21
DIMMA_ODT0	J14-116	U22-AL23
DIMMA_ODT1	J14-120	U22-AK23
DIMMA_RASN	J14-110	U22-AN22
DIMMA_RSTN	J14-30	U22-AL13
DIMMA_WEN	J14-113	U22-AM27
SODIMM B (J21) – FPGA B (U24)		
DIMMB_A0	J21-98	U24-C18
DIMMB_A1	J21-97	U24-L16
DIMMB_A10	J21-107	U24-A15
DIMMB_A11	J21-84	U24-A28
DIMMB_A12	J21-83	U24-F20
DIMMB_A13	J21-119	U24-D12
DIMMB_A14	J21-80	U24-D30
DIMMB_A15	J21-78	U24-C30
DIMMB_A2	J21-96	U24-B18
DIMMB_A3	J21-95	U24-B16
DIMMB_A4	J21-92	U24-D22
DIMMB_A5	J21-91	U24-A19

Signal Name	SODIMM	FPGA
DIMMB_A6	J21-90	U24-C22
DIMMB_A7	J21-86	U24-A29
DIMMB_A8	J21-89	U24-A18
DIMMB_A9	J21-85	U24-C19
DIMMB_BA0	J21-109	U24-B15
DIMMB_BA1	J21-108	U24-D15
DIMMB_BA2	J21-79	U24-B30
DIMMB_CASN	J21-115	U24-M13
DIMMB_CK_FBN	U24-G20	U24-L21
DIMMB_CK_FBP	U24-F21	U24-L20
DIMMB_CK0N	J21-103	U24-E24
DIMMB_CK0P	J21-101	U24-D24
DIMMB_CK1N	J21-104	U24-J14
DIMMB_CK1P	J21-102	U24-K14
DIMMB_CKE0	J21-73	U24-D27
DIMMB_CKE1	J21-74	U24-G25
DIMMB_DM0	J21-11	U24-F28
DIMMB_DM1	J21-28	U24-B31
DIMMB_DM2	J21-46	U24-J20
DIMMB_DM3	J21-63	U24-H22
DIMMB_DM4	J21-136	U24-J17
DIMMB_DM5	J21-153	U24-L19
DIMMB_DM6	J21-170	U24-G12
DIMMB_DM7	J21-187	U24-J11
DIMMB_DQ0	J21-5	U24-C24
DIMMB_DQ1	J21-7	U24-C25
DIMMB_DQ10	J21-33	U24-B27
DIMMB_DQ11	J21-35	U24-C27
DIMMB_DQ12	J21-22	U24-G26
DIMMB_DQ13	J21-24	U24-G27
DIMMB_DQ14	J21-34	U24-B26
DIMMB_DQ15	J21-36	U24-A26

Signal Name	SODIMM	FPGA
DIMMB_DQ16	J21-39	U24-B23
DIMMB_DQ17	J21-41	U24-C23
DIMMB_DQ18	J21-51	U24-C20
DIMMB_DQ19	J21-53	U24-D20
DIMMB_DQ2	J21-15	U24-B25
DIMMB_DQ20	J21-40	U24-A23
DIMMB_DQ21	J21-42	U24-A24
DIMMB_DQ22	J21-50	U24-G21
DIMMB_DQ23	J21-52	U24-G22
DIMMB_DQ24	J21-57	U24-B21
DIMMB_DQ25	J21-59	U24-B22
DIMMB_DQ26	J21-67	U24-E19
DIMMB_DQ27	J21-69	U24-D19
DIMMB_DQ28	J21-56	U24-E22
DIMMB_DQ29	J21-58	U24-E23
DIMMB_DQ3	J21-17	U24-A25
DIMMB_DQ30	J21-68	U24-A20
DIMMB_DQ31	J21-70	U24-A21
DIMMB_DQ32	J21-129	U24-F18
DIMMB_DQ33	J21-131	U24-E17
DIMMB_DQ34	J21-141	U24-H17
DIMMB_DQ35	J21-143	U24-G17
DIMMB_DQ36	J21-130	U24-K18
DIMMB_DQ37	J21-132	U24-K17
DIMMB_DQ38	J21-140	U24-E18
DIMMB_DQ39	J21-142	U24-D17
DIMMB_DQ4	J21-4	U24-D25
DIMMB_DQ40	J21-147	U24-M18
DIMMB_DQ41	J21-149	U24-M17
DIMMB_DQ42	J21-157	U24-E16
DIMMB_DQ43	J21-159	U24-D16
DIMMB_DQ44	J21-146	U24-K19

Signal Name	SODIMM	FPGA
DIMMB_DQ45	J21-148	U24-J19
DIMMB_DQ46	J21-158	U24-C17
DIMMB_DQ47	J21-160	U24-B17
DIMMB_DQ48	J21-163	U24-D14
DIMMB_DQ49	J21-165	U24-C14
DIMMB_DQ5	J21-6	U24-D26
DIMMB_DQ50	J21-175	U24-G11
DIMMB_DQ51	J21-177	U24-F11
DIMMB_DQ52	J21-164	U24-G13
DIMMB_DQ53	J21-166	U24-H14
DIMMB_DQ54	J21-174	U24-A13
DIMMB_DQ55	J21-176	U24-A14
DIMMB_DQ56	J21-181	U24-H12
DIMMB_DQ57	J21-183	U24-J12
DIMMB_DQ58	J21-191	U24-H10
DIMMB_DQ59	J21-193	U24-G10
DIMMB_DQ6	J21-16	U24-E26
DIMMB_DQ60	J21-180	U24-F14
DIMMB_DQ61	J21-182	U24-E14
DIMMB_DQ62	J21-192	U24-B12
DIMMB_DQ63	J21-194	U24-B13
DIMMB_DQ7	J21-18	U24-F26
DIMMB_DQ8	J21-21	U24-H27
DIMMB_DQ9	J21-23	U24-G28
DIMMB_DQS0N	J21-10	U24-B28
DIMMB_DQS0P	J21-12	U24-C28
DIMMB_DQS1N	J21-27	U24-H29
DIMMB_DQS1P	J21-29	U24-H28
DIMMB_DQS2N	J21-45	U24-H20
DIMMB_DQS2P	J21-47	U24-H19
DIMMB_DQS3N	J21-62	U24-K22
DIMMB_DQS3P	J21-64	U24-K21

Signal Name	SODIMM	FPGA
DIMMB_DQS4N	J21-135	U24-L14
DIMMB_DQS4P	J21-137	U24-L15
DIMMB_DQS5N	J21-152	U24-J15
DIMMB_DQS5P	J21-154	U24-H15
DIMMB_DQS6N	J21-169	U24-M11
DIMMB_DQS6P	J21-171	U24-M12
DIMMB_DQS7N	J21-186	U24-B11
DIMMB_DQS7P	J21-188	U24-A11
DIMMB_EVENTN	J21-198	U24-D11
DIMMB_NC0	J21-77	U24-A30
DIMMB_NC2	J21-122	U24-M16
DIMMB_NC3	J21-125	U24-M15
DIMMB_ODT0	J21-116	U24-F15
DIMMB_ODT1	J21-120	U24-E13
DIMMB_RASN	J21-110	U24-C15
DIMMB_RSTN	J21-30	U24-A31
DIMMB_WEN	J21-113	U24-C12

3.4.8 DDR3 PCB Trace Lengths

The DDR3 traces on the DN-DualV6-PCIe-4 Logic Emulation Board are routed to the following lengths refer to Table 25:

Table 25 – DDR3 PCB Trace Lengths

Signal Name	Routed Length (mm)	Description
DIMMA_CK0N	60.11	Clock group
DIMMA_A0	60.05	Control group
DIMMA_DQ0	70.06	Data byte group
DIMMB_CK0N	76.03	Clock group
DIMMB_A0	76.91	Control group
DIMMB_DQ0	76.00	Data byte group

3.5 SATA Interface on FPGA A and FPGA B

Serial ATA is a high-speed serial link replacement for the parallel ATA attachment of mass storage devices. The serial link employed is a high-speed differential layer that utilizes gigabit technology and 8b/10b encoding. Two SATA II compliant ports, one configured as a HOST, and the other as a Device, is provided on FPGA A and FPGA B, see Figure 22. Both TX/RX signal pairs are differentially routed and AC-coupled with 0.1uF capacitors.

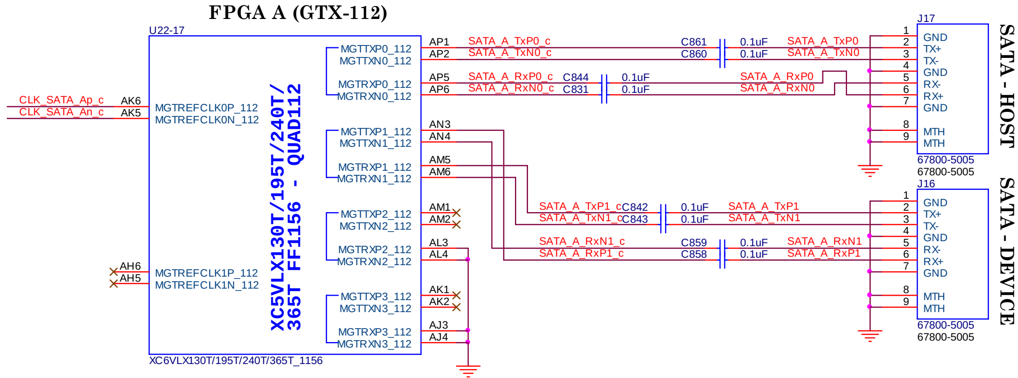


Figure 22 - SATA Interface on FPGA A

The two SATA II ports connects directly to the FPGA A and FPGA B, see Table 26.

Table 26 – SATA II Ports on FPGA A and FPGA B

Signal Name	FPGA	SATA
SATA_A_TxP0	U22-AP1	J17.2
SATA_A_TxN0	U22-AP2	J17.3
SATA_A_RxP0	U22-AP5	J17.6
SATA_A_RxN0	U22-AP6	J17.5
SATA_A_TxP1	U22-AM5	J16.2
SATA_A_TxN1	U22-AM6	J16.3
SATA_A_RxP1	U22-AN3	J16.6
SATA_A_RxN1	U22-AN4	J16.5
SATA_B_TxP0	U24-D1	J18.2
SATA_B_TxN0	U24-D2	J18.3
SATA_B_RxP0	U24-G3	J18.6
SATA_B_RxN0	U24-G4	J18.5
SATA_B_TxP1	U24-E3	J19.2
SATA_B_TxN1	U24-E4	J19.3

Signal Name	FPGA	SATA
SATA_B_RxP1	U24-C3	J19.6
SATA_B_RxN1	U24-C4	J19.5

3.6 Interconnect - FPGA A to FPGA B

3.6.1 High-speed (LVDS) IO Bus

Four high-speed (LVDS) IO Banks are connected between the FPGA A and FPGA B. Table 27 shows the connection between the FPGA A and FPGA B.

Table 27 – High-speed (LVDS) IO Bus between FPGA A and FPGA B

Signal Name	FPGA A	FPGA B
AB0N0	U22-A31	U24-AH32
AB0N1	U22-D30	U24-AD26
AB0N10	U22-F26	U24-AM31
AB0N11	U22-D26	U24-AK31
AB0N12	U22-C25	U24-AK34
AB0N13	U22-G25	U24-AL33
AB0N14	U22-E24	U24-AM32
AB0N15	U22-B28	U24-AP33
AB0N16	U22-D29	U24-AE26
AB0N17	U22-A25	U24-AN34
AB0N18	U22-E28	U24-AG30
AB0N19	U22-H29	U24-AG28
AB0N2	U22-F29	U24-AF29
AB0N3	U22-A29	U24-AH30
AB0N4	U22-C27	U24-AH34
AB0N5	U22-A26	U24-AK32
AB0N6	U22-B30	U24-AD27
AB0N7	U22-E27	U24-AE29
AB0N8	U22-G28	U24-AJ32
AB0N9	U22-G27	U24-AJ30
AB0P0	U22-B31	U24-AH33
AB0P1	U22-C30	U24-AD25
AB0P10	U22-E26	U24-AL30

Signal Name	FPGA A	FPGA B
AB0P11	U22-D25	U24-AL31
AB0P12	U22-C24	U24-AL34
AB0P13	U22-F25	U24-AM33
AB0P14	U22-D24	U24-AN32
AB0P15	U22-C28	U24-AP32
AB0P16	U22-C29	U24-AF26
AB0P17	U22-B25	U24-AN33
AB0P18	U22-F28	U24-AF30
AB0P19	U22-H28	U24-AG27
AB0P2	U22-E29	U24-AF28
AB0P3	U22-A28	U24-AH29
AB0P4	U22-B27	U24-AJ34
AB0P5	U22-B26	U24-AK33
AB0P6	U22-A30	U24-AE27
AB0P7	U22-D27	U24-AE28
AB0P8	U22-H27	U24-AJ31
AB0P9	U22-G26	U24-AJ29
AB1N0	U22-J22	U24-AD20
AB1N1	U22-L21	U24-AD19
AB1N10	U22-A21	U24-AN18
AB1N11	U22-C23	U24-AN20
AB1N12	U22-A24	U24-AN23
AB1N13	U22-G20	U24-AD21
AB1N14	U22-H20	U24-AG21
AB1N15	U22-F20	U24-AH20
AB1N16	U22-K22	U24-AE19
AB1N17	U22-J21	U24-AF21
AB1N18	U22-E23	U24-AL19
AB1N19	U22-C19	U24-AP21
AB1N2	U22-G22	U24-AH22
AB1N3	U22-D22	U24-AL23
AB1N4	U22-E21	U24-AL21

Signal Name	FPGA A	FPGA B
AB1N5	U22-D20	U24-AJ22
AB1N6	U22-D19	U24-AJ21
AB1N7	U22-C18	U24-AL20
AB1N8	U22-B22	U24-AN22
AB1N9	U22-A19	U24-AL18
AB1P0	U22-H22	U24-AC20
AB1P1	U22-L20	U24-AC19
AB1P10	U22-A20	U24-AP19
AB1P11	U22-B23	U24-AN19
AB1P12	U22-A23	U24-AP22
AB1P13	U22-F21	U24-AE21
AB1P14	U22-H19	U24-AG20
AB1P15	U22-F19	U24-AJ20
AB1P16	U22-K21	U24-AF19
AB1P17	U22-J20	U24-AF20
AB1P18	U22-E22	U24-AK19
AB1P19	U22-B20	U24-AP20
AB1P2	U22-G21	U24-AG22
AB1P3	U22-C22	U24-AM23
AB1P4	U22-D21	U24-AM21
AB1P5	U22-C20	U24-AK22
AB1P6	U22-E19	U24-AK21
AB1P7	U22-B18	U24-AM20
AB1P8	U22-B21	U24-AM22
AB1P9	U22-A18	U24-AM18
AB2N0	U24-AN14	U22-A14
AB2N1	U24-AM13	U22-C14
AB2N10	U24-AL10	U22-G10
AB2N11	U24-AL13	U22-F11
AB2N12	U24-AK11	U22-H13
AB2N13	U24-AJ12	U22-J14
AB2N14	U24-AC14	U22-M13

Signal Name	FPGA A	FPGA B
AB2N15	U24-AH14	U22-M11
AB2N16	U24-AP12	U22-C12
AB2N17	U24-AH10	U22-H14
AB2N18	U24-AD11	U22-K12
AB2N2	U24-AF14	U22-E14
AB2N3	U24-AG13	U22-F13
AB2N4	U24-AG10	U22-J10
AB2N5	U24-AE12	U22-J12
AB2N6	U24-AE11	U22-L11
AB2N7	U24-AH12	U22-B11
AB2N8	U24-AN12	U22-B13
AB2N9	U24-AM11	U22-E12
AB2P0	U24-AP14	U22-A13
AB2P1	U24-AN13	U22-D14
AB2P10	U24-AM10	U22-H10
AB2P11	U24-AK13	U22-G11
AB2P12	U24-AJ11	U22-G12
AB2P13	U24-AK12	U22-K14
AB2P14	U24-AD14	U22-L13
AB2P15	U24-AH13	U22-M12
AB2P16	U24-AP11	U22-C13
AB2P17	U24-AJ10	U22-G13
AB2P18	U24-AD12	U22-K13
AB2P2	U24-AE14	U22-F14
AB2P3	U24-AF13	U22-E13
AB2P4	U24-AG11	U22-J11
AB2P5	U24-AE13	U22-H12
AB2P6	U24-AF11	U22-K11
AB2P7	U24-AG12	U22-A11
AB2P8	U24-AM12	U22-B12
AB2P9	U24-AL11	U22-D12
AB3N0	U22-F15	U24-AH19

Signal Name	FPGA A	FPGA B
AB3N1	U22-J16	U24-AF15
AB3N10	U22-G17	U24-AK16
AB3N11	U22-G16	U24-AJ14
AB3N12	U22-J15	U24-AH15
AB3N13	U22-K17	U24-AJ16
AB3N14	U22-B16	U24-AF18
AB3N15	U22-L16	U24-AF16
AB3N16	U22-H18	U24-AG17
AB3N17	U22-L14	U24-AD16
AB3N18	U22-M15	U24-AD15
AB3N19	U22-M17	U24-AC17
AB3N2	U22-J19	U24-AG18
AB3N3	U22-L18	U24-AE17
AB3N4	U22-E17	U24-AK17
AB3N5	U22-D17	U24-AP17
AB3N6	U22-D16	U24-AP15
AB3N7	U22-B17	U24-AM16
AB3N8	U22-B15	U24-AM15
AB3N9	U22-C15	U24-AL14
AB3P0	U22-G15	U24-AJ19
AB3P1	U22-J17	U24-AG15
AB3P10	U22-H17	U24-AL16
AB3P11	U22-F16	U24-AK14
AB3P12	U22-H15	U24-AJ15
AB3P13	U22-K18	U24-AJ17
AB3P14	U22-A16	U24-AE18
AB3P15	U22-K16	U24-AG16
AB3P16	U22-G18	U24-AH17
AB3P17	U22-L15	U24-AE16
AB3P18	U22-M16	U24-AC15
AB3P19	U22-M18	U24-AC18
AB3P2	U22-K19	U24-AH18

Signal Name	FPGA A	FPGA B
AB3P3	U22-L19	U24-AD17
AB3P4	U22-F18	U24-AK18
AB3P5	U22-E18	U24-AN17
AB3P6	U22-E16	U24-AP16
AB3P7	U22-C17	U24-AM17
AB3P8	U22-A15	U24-AN15
AB3P9	U22-D15	U24-AL15

3.6.2 High-Speed Interconnect (GTP) Configuration FPGA to FPGA A/B

Two high-speed serial channels are provided between the Configuration FPGA and FPGA A/B. This could be used for pin multiplexing, 10x pin per LVDS pair. The GTP transceiver is highly configurable and tightly integrated with the programmable logic resources of the FPGA. It provides the following features to support a wide variety of applications:

- Current Mode Logic (CML) serial drivers/buffers with configurable termination, voltage swing, and coupling
- Programmable TX pre-emphasis and RX equalization for optimized signal integrity
- Line rates from 100 Mb/s to 3.75 Gb/s, with optional 5x digital oversampling required for rates between 100 Mb/s and 500 Mb/s
- Optional built-in PCS features, such as 8B/10B encoding, comma alignment, channel bonding, and clock correction
- Fixed latency modes for minimized, deterministic datapath latency
- Beacon signaling for PCI Express designs and Out-of-Band signaling including
- COM signal support for SATA designs

The Xilinx CORE Generator tool includes a Wizard to automatically configure GTP transceivers to support one of various protocols or perform custom configuration (see "*UG-198 – Virtex-5 RocketIO GTX Transceiver User Guide*").

GTP transceivers are placed as dual transceiver GTP_DUAL tiles in Virtex-5 LXT and SXT Platform devices. This configuration allows two transceivers to share a single PLL with the TX and RX functions of both, reducing size and power consumption.

Table 18 shows the connection between the Configuration FPGA and FPGA A/B. In-line AC-Coupling capacitors are provided for DC isolation from the Transmitter.

Table 28 – High-Speed Serial connection between the Configuration FPGA and FPGA A/B

Signal Name	Configuration FPGA	FPGA A/B
HS_CF_A_TXP0	U17-AK2	U22-G3
HS_CF_A_TXN0	U17-AL2	U22-G4
HS_CF_A_RXP0	U17-AL1	U22-D1
HS_CF_A_RXN0	U17-AM1	U22-D2
HS_CF_A_TXP1	U17-AN4	U22-E3
HS_CF_A_TXN1	U17-AN3	U22-E4
HS_CF_A_RXP1	U17-AP3	U22-C3
HS_CF_A_RXN1	U17-AP2	U22-C4
HS_CF_B_TXP0	U17-AD2	U24-AP5
HS_CF_B_TXN0	U17-AE2	U24-AP6
HS_CF_B_RXP0	U17-AE1	U24-AP1
HS_CF_B_RXN0	U17-AF1	U24-AP2
HS_CF_B_TXP1	U17-AJ2	U24-AM5
HS_CF_B_TXN1	U17-AH2	U24-AM6
HS_CF_B_RXP1	U17-AH1	U24-AN3
HS_CF_B_RXN1	U17-AG1	U24-AN4

3.7 Backup Battery

The encryption key memory cells are volatile and must receive continuous power to retain their contents. During normal operation, these memory cells are powered by the auxiliary voltage input (VCCAUX), although a separate VBATT power input is provided for retaining the key when VCCAUX is removed. Because VBATT draws very little current (on the order of nanoamperes), a small watch battery is suitable for this supply. (To estimate the battery life, refer to *DS152 - Virtex-6 FPGA Data Sheet - DC and Switching Characteristics.* At less than a 100 nA load, the endurance of the battery should be limited only by its shelf life. VBATT does not draw any current and can be removed while VCCAUX is applied. VBATT cannot be used for any purpose other than retaining the encryption keys when VCCAUX is removed.

In addition to supplying the power for FPGAs, the backup battery (BT1) also provides power for the Real Time Clock (U36). Backup Batteries are available Panasonic, Lithium Coin Cell, 3V 40mAH from Digi-Key, P/N CR1220.

3.7.1 Backup Battery Circuit

The recommended battery voltage is specified at +1.0V to +2.5V. The TPS782 low-dropout regulator (LDOs) offers the benefits of ultra-low power (I_Q = 1μA), see Figure 23.

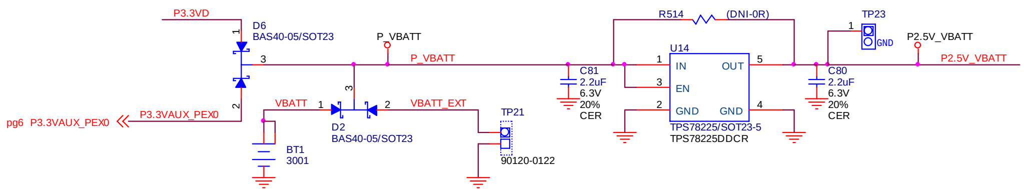


Figure 23 - Backup Battery Supply

3.7.2 Backup Battery Loads

The backup battery supplies the following loads, see Table 29.

Table 29 – Backup Battery Loads

Signal Name	Load	Description
P2.5V_VBATT	U22-N8	FPGA A
P2.5V_VBATT	U24-N8	FPGA B
P_VBATT	U17-L23	Configuration FPGA
P_VBATT	U36-3	Real Time Clock (RTC)

3.8 VCCINT Switching Power Supply (FPGA A/B)

The PTH08T250W is a high-performance 50-A rated, non-isolated power module operating from an input voltage range of 4.5 V to 14 V. The PTH08T250W requires a single resistor (R183) to set the output voltage to +1.0V. FPGA A/B share a single PTH08T250W supply between both FPGAs, see Figure 24.

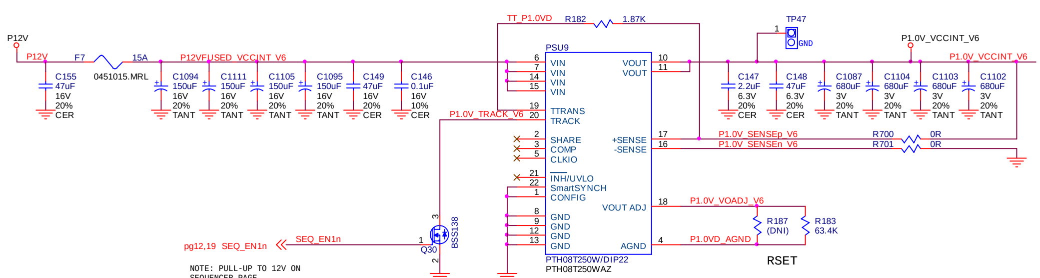


Figure 24 – VCCINT Switching Supply for FPGA A/B

Note: In order to comply with the PCI Express Mechanical requirements, the VCCINT power supply was designed to meet the "nominal" power requirements of FPGA A/B. Power and heat sinking on FPGA A/B was compromised and the user design may exceed the requirements under worst-case conditions.

4 Clock Generation

4.1 Clock Methodology

The DN-DualV6-PCIe-4 has a flexible and configurable clocking scheme. Figure 25 is a block diagram showing the clocking resources and connections. All of the "Global Clock Networks" on the DN-DualV6-PCIe-4 are routed point-to-point using dedicated LVDS routes. Since LVDS is a low voltage-swing differential signal, using a single ended input buffer in the FPGA will not work. An example Verilog implementation of a differential clock input is given below:

```
IBUFGDS # (.DIFF_TERM("TRUE")) CLK0_IBUFGi (.O(clk0_ibufg), .I(CLK_G0P), .IB(CLK_G0N));
```

The pin assignment in the UCF file:

```
NET "CLK_G0N" loc =M22;

NET "CLK_G0P" loc =L23;
```

All global clock networks have a differential test point terminated by a 100R resistor used to measure clock frequency e.g. TP19. The positive side of the differential signal is connected to pin 1 (square) and the negative side is connected to pin 2 (circular) of the test point.

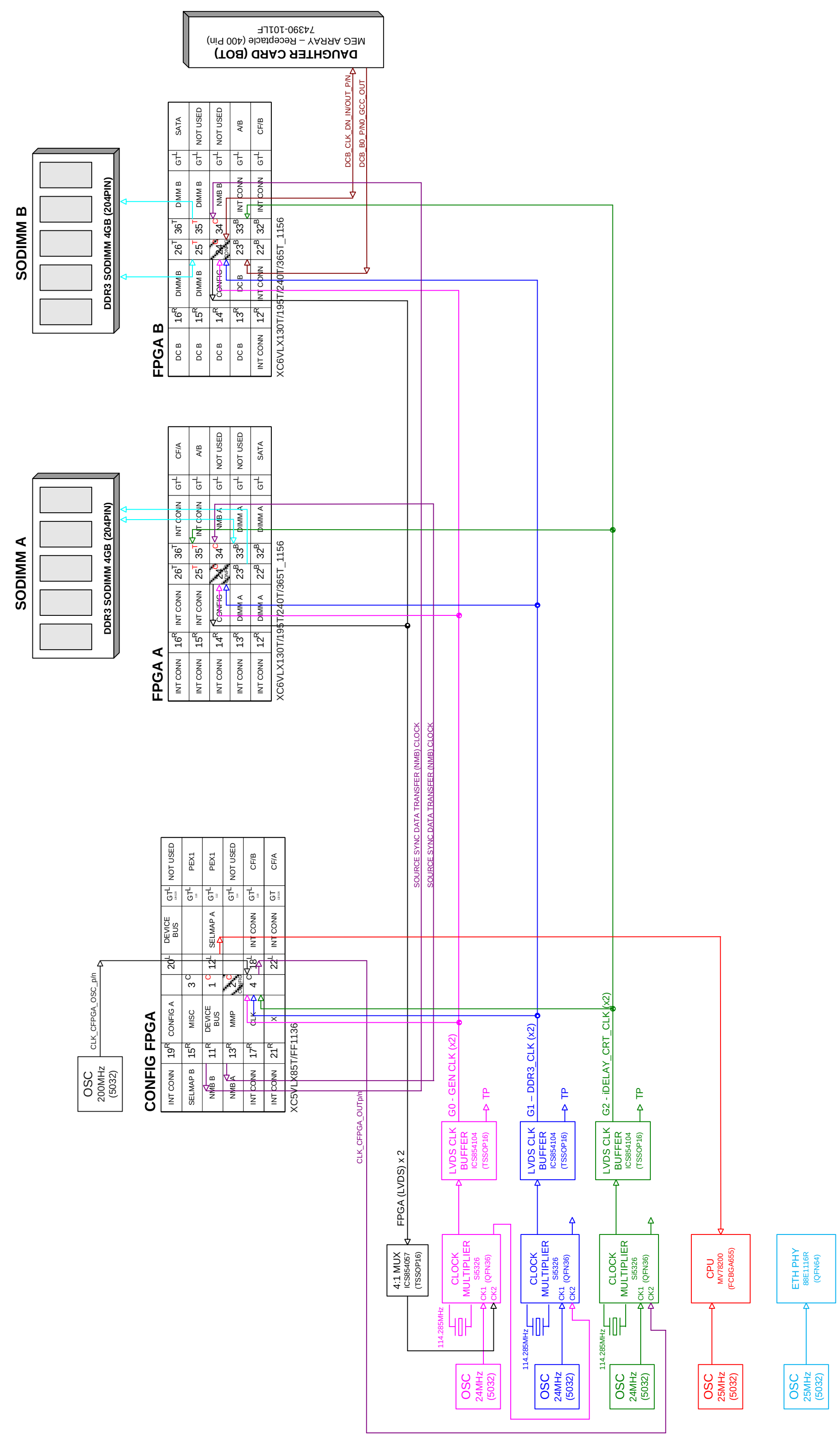


Figure 25 - Clocking Block Diagram

- FPGA Clock Multipliers – Si5326 (x3)
  - General Clock Multiplier (U10) - CLK_G0
  - DDR2 Clock Multiplier (U16) – CLK_G1
  - LVDS Clock Multiplier (U20) - CLK_G2
- Multiplexed Global clocks from FPGA A/B
- PCI Express Reference Clock
- Oscillators for GTP Transceivers (x4)
- Daughter Card Header Clocks
  - DCA_CLK_DN_IN_P/N
  - DCA_CLK_UP_OUT_P/N
- Not Main Bus (NMB) Clock – Source Synchronous
- External Clock Input – CLK_MUX_TPp/n (not shown in block diagram)

The individual clock resources will be further explained in the following paragraphs.

4.2 Clock Multipliers (x3)

The Si5326 is a jitter-attenuating precision clock multiplier for applications requiring sub 1 ps jitter performance. The Si5326 accepts dual clock inputs ranging from 2 kHz to 710 MHz and generates two clock outputs ranging from 2 kHz to 945 MHz and select frequencies to 1.4 GHz. The two outputs are divided down separately from a common source. The device provides virtually any frequency translation combination across this operating range. The Si5326 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface (configured for I^2C). The Si5326 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Please refer to the "*Any-rate Precision Clocks Si5316, Si5322, Si5323, Si5325, Si5326, Si5365, Si5366, Si5367, Si5368 Family Reference Manual*" from Silicon Laboratories for the Si5326 for programming information.

4.2.1 General Clock Multiplier (U10) - CLK_G0

One of the outputs of the Clock Multiplier (U10) is buffered (U9) and distributed as a general reference clock for the FPGAs while the other output is connected to the "CKIN2" input on the DDR3 CLK Multiplier (U16). The clock multiplier (U10) can use either oscillator (X1) or FPGA A/B clock output signals (multiplexed) as a reference input. The clock multiplier (U10) must be programmed via the I^2C interface. Signal

> Note: Three clock multipliers (U10, U16, and U20) are on the I^2C chain, driven from the Configuration FPGA (U17).

"RST_SYNTH_G0/1/2n" are provided to reset the clock multiplier.

Figure 26 shows one of the clock multiplier circuits. LED (DS7) is used to indicate "PLL Loss of Lock".

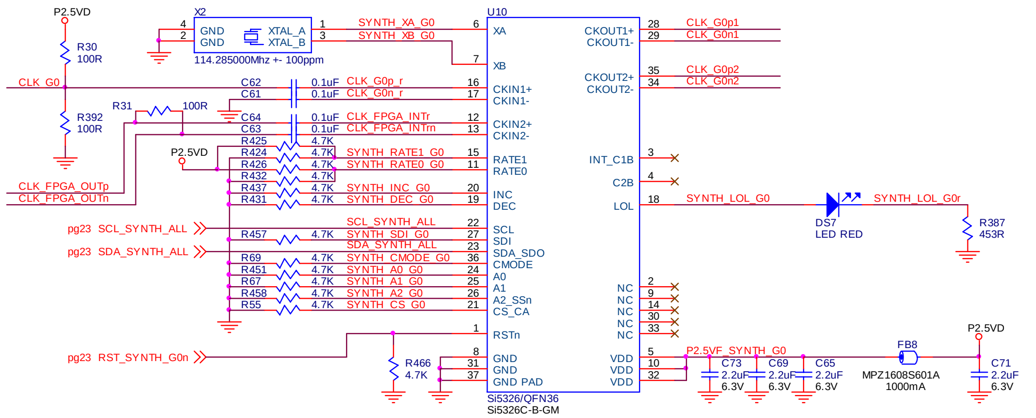


Figure 26 - Clock Multiplier Circuit – CLK_G0

4.2.2 Connections between the FPGAs and Clock Multipliers

All of the "Global Clock Networks" on the DN-DualV6-PCIe-4 are routed point-to-point using dedicated differential (LVDS) traces. The arrival times of the clock edges at each FPGA are phase-aligned (length-matched on the PCB) within about 100ps. These clocks are all suitable for synchronous communication among FPGAs. The connections between the FPGAs and the Clock Multipliers are shown in Table 30.

Table 30 - Connections between FPGAs and Clock Multipliers

Signal Name	Clock Buffer	FPGA
General Clock Multiplier (CLK_G0)		
CLK_G0_AN	U9-13	U22-M22
CLK_G0_AP	U9-14	U22-L23
CLK_G0_BN	U9-11	U24-M22
CLK_G0_BP	U9-12	U24-L23
CLK_G0_CFPGAN	U9-9	U17-AG13
CLK_G0_CFPGAP	U9-10	U17-AH12
CLK_G0_TN	U9-15	TP19-2
CLK_G0_TP	U9-16	TP19-1
DDR2 Clock Multiplier (CLK_G1)		
CLK_G1_AN	U15-13	U22-K23

Signal Name	Clock Buffer	FPGA
CLK_G1_AP	U15-14	U22-K24
CLK_G1_BN	U15-11	U24-K23
CLK_G1_BP	U15-12	U24-K24
CLK_G1_CFPGAN	U15-9	U17-AH19
CLK_G1_CFPGAP	U15-10	U17-AH20
CLK_G1_TN	U15-15	TP25-2
CLK_G1_TP	U15-16	TP25-1
LVDS Clock Multiplier (CLK_G2)		
CLK_G2_AN	U19-13	U22-E11
CLK_G2_AP	U19-14	U22-D11
CLK_G2_BN	U19-11	U24-AC12
CLK_G2_BP	U19-12	U24-AC13
CLK_G2_CFPGAN	U19-9	U17-AH13
CLK_G2_CFPGAP	U19-10	U17-AH14
CLK_G2_TN	U19-15	TP29-2
CLK_G2_TP	U19-16	TP29-1

Note: The maximum, clock frequency with the ICS854104 differential-to-LVDS clock buffers are 700MHz, see datasheet.

4.3 Multiplexed Global Clocks from FPGA A/B

The ICS854057 is a 4:1 LVDS Clock Multiplexer which can operate up to 2GHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The CLKp, CLKn pairs can accept most standard differential input levels. Internal termination is provided on each differential input pair. The ICS854057 operates using a +2.5V supply voltage. The fully differential architecture and low propagation delay make it ideal for use in high speed multiplexing applications. The select pins have internal pull-down resistors.

4.3.1 Multiplexed Global Clock Circuit

CLK_FPGAA_OUTp/n and CLK_FPGAB_OUTp/n are LVDS clock outputs from FPGA A/B that are multiplexed by the ICS854057 (U6) and allow the G0 clock network to be driven by either FPGA A, or FPGA B, see Figure 27.

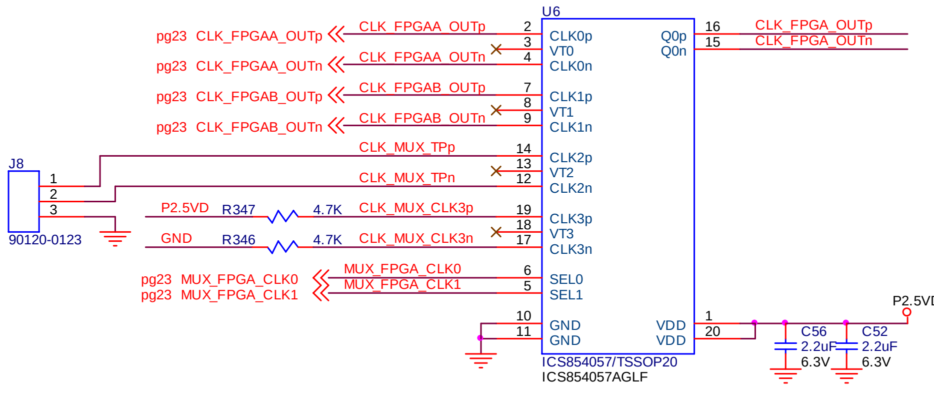


Figure 27 - Multiplexed Global Clocks from FPGA A/B

4.3.2 Connection between FPGA A/B and the Clock Multiplexer

The connection between FPGA A/B and the Clock Multiplexer (U6) are shown in Table 31.

Table 31 - Connection between FPGA A/B and Clock Multiplexer

Signal Name	FPGA A/B	Clock MUX 4:1
CLK_FPGAA_OUTp	U22-M23	U6-2
CLK_FPGAA_OUTn	U22-L24	U6-4
CLK_FPGAB_OUTp	U27-F24	U6-7
CLK_FPGAB_OUTn	U27-F23	U6-9
CLK_MUX_TPp	J8-1	U6-14
CLK_MUX_TPn	J8-2	U6-12
MUX_FPGA_CLK0	U17-T10	U6-6
MUX_FPGA_CLK1	U17-T11	U6-5

4.4 PCI Express Reference Clocks

In-system, the PCI Express clock from the PCI Express Edge connector drives the Marvell MV78200 PEX0 port directly. The ICS557-05A is provided as a clock source for the backend, to drive the PEX1 port and the Configuration FPGA GTP Transceivers. The ICS5507-05A provides the HCSL clocks for the backend. The ICS557-05A is a spread-spectrum clock generator that supports PCI-Express requirements. It is used in PC or embedded systems to substantially reduce electro-magnetic interference (EMI). The device provides four differential HCSL or LVDS high-frequency outputs with spread spectrum capability. The output frequency and spread type are selectable using external pins.

4.4.1 PCI Express Reference Clock Circuit

The PCI Express clock buffer (U13) is provided to distribute the clock network to the Marvell MV78200 PEX1 port and the Configuration FPGA GTP Transceivers, see Figure 28.

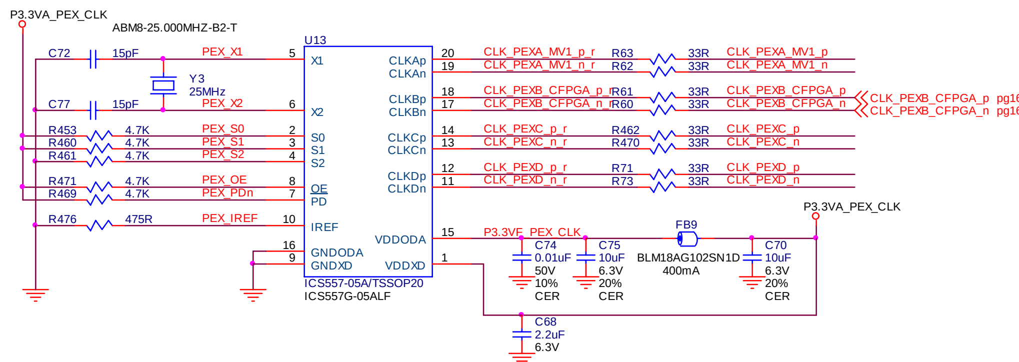


Figure 28 – PCI Express Reference Clock Circuit

4.4.2 Connection between CPU/CF FPGA and the PCIe Reference Clock Buffer

The connection between the Marvell MV78200/Configuration FPGA and the PCIe Reference Clock Buffer (U13) are shown in Table 32. These signals are routed as differential pairs (LVDS) and are AC-coupled.

Table 32 - Connection between CPU/Configuration FPGA and PCI Express Reference Clock Buffer

Signal Name	PCI Express Edge Connector	CPU
CLK_PEX0_p0	P1-A13	U4-W1
CLK_PEX0_n0	P1-A14	U4-Y1
Signal Name	**Clock Buffer**	**CPU/CF FPGA**
CLK_PEXA_MV1_p	U13-20	U4-AC1
CLK_PEXA_MV1_n	U13-19	U4-AB1
CLK_PEXB_CFPGA_p	U13-18	U17-H4
CLK_PEXB_CFPGA_n	U13-17	U17-H3

4.5 GTP Clock (LVDS) Oscillators and Buffers (x4)

The differential oscillators (X9, X11, X10 and X12) is powered from +2.5V, and provides a differential reference clock to the GTP Transceivers, see Figure 29. The GTP Clock Oscillators are assigned as follows:

- X9 – High-speed SERDES links between Configuration FPGA and FPGA A/B

- X11 - High-speed SERDES links between FPGA A and FPGA B
- X10 – SATA II Oscillator for FPGA A
- X12 – SATA II Oscillator for FPGA B

The Silicon Laboratories Si534 Quad Frequency Crystal Oscillator is recommended for this application and is available in frequencies from 10MHz to 945MHz. The default factory installed oscillator is running at 312.5MHz. They are available from Nu Horizons, P/N: 534FB000184DG. The oscillator is pre-programmed to four fixed frequencies, and the output is selected based on the value of "OSC_CFV6_FS1/0" signals, see Table 33. Reference the schematic for more information.

Table 33 - GTP Oscillator Frequency Select Signals

Frequency Select	Value	Frequency (MHz)
OSC_CFV6_FS[1..0]	00	156.25
OSC_CFV6_FS[1..0]	01	200.00
OSC_CFV6_FS[1..0]	10	250.00
OSC_CFV6_FS[1..0]	11	312.50
OSC_AB_FS [1..0]	00	156.25
OSC_AB_FS [1..0]	01	200.00
OSC_AB_FS [1..0]	10	250.00
OSC_AB_FS [1..0]	11	312.50
OSC_SATA_A_FS [1..0]	00	x
OSC_SATA_A_FS [1..0]	01	x
OSC_SATA_A_FS [1..0]	10	x
OSC_SATA_A_FS [1..0]	11	x
OSC_SATA_B_FS [1..0]	00	x
OSC_SATA_B_FS [1..0]	01	x
OSC_SATA_B_FS [1..0]	10	x
OSC_SATA_B_FS [1..0]	11	x

Note: Fixed frequency 150MHz oscillators are provided for X10, and X12, P/N LV7745DW-150.0M.

4.5.1 GTP Clock Oscillator - Configuration FPGA and FPGA A/B

The ICS854104 (U23) is a low skew, high performance 1-to-4 Differential-to-LVDS Clock Fanout Buffer that is driven by the Si534 Quad Frequency Crystal Oscillator (X9), see Figure 29.

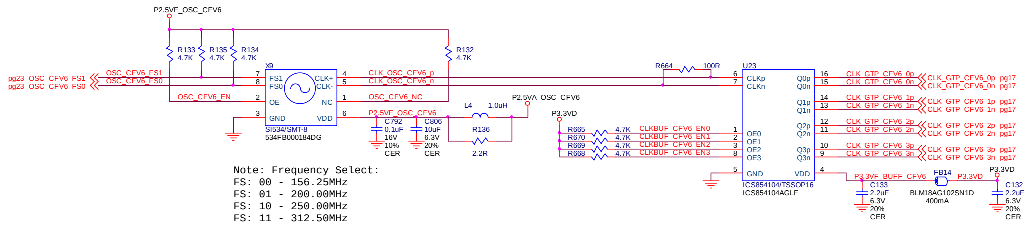


Figure 29 – GTP Clock Oscillator and Buffer

4.5.2 Connection between GTP Clock Buffers and the FPGAs

The connections between the GTP Clock Buffers and the FPGAs are shown in Table 34. These signals are routed as differential pairs (LVDS) and are AC-coupled.

Table 34 - Connection between GTP Clock Buffers and FPGAs

Signal Name	Clock Buffer	FPGA A/B
CLK_GTP_CFV6_0P	U23-16	U17-AF4
CLK_GTP_CFV6_0N	U23-15	U17-AF3
CLK_GTP_CFV6_1P	U23-14	U17-AL5
CLK_GTP_CFV6_1N	U23-13	U17-AL4
CLK_GTP_CFV6_2P	U23-12	U22-H6
CLK_GTP_CFV6_2N	U23-11	U22-H5
CLK_GTP_CFV6_3P	U23-10	U24-AK6
CLK_GTP_CFV6_3N	U23-9	U24-AK5
Signal Name	**Clock Buffer**	**CPU/CF FPGA**
CLK_GTX_AB_0P	U59-16	U22-P6
CLK_GTX_AB_0N	U59-15	U22-P5
CLK_GTX_AB_1P	U59-14	U24-AD6
CLK_GTX_AB_1N	U59-13	U24-AD5

The oscillator power supply (U60) is filtered to reduce power supply noise and jitter. Please see the Si534 datasheet for more information.

4.5.3 GTP Clock Oscillator - FPGA A and FPGA B

The ICS854104 (U59) is a low skew, high performance 1-to-4 Differential-to-LVDS Clock Fanout Buffer that is driven by the Si534 Quad Frequency Crystal Oscillator (X11), see Figure 30.

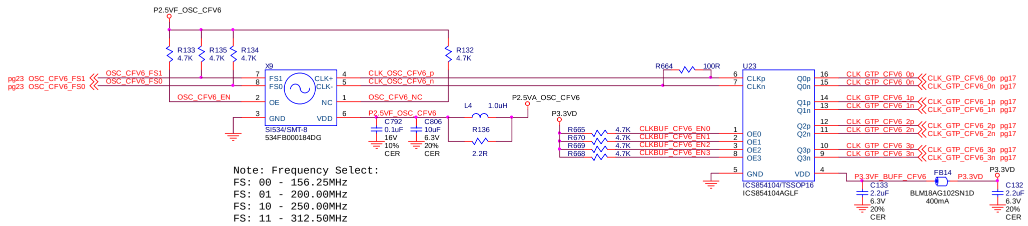


Figure 30 – GTP Clock Oscillator and Buffer

4.5.4 Connection between GTP Clock Buffer and FPGA A/B

The connections between the GTP Clock Buffers and FPGA A/B are shown in Table 35. These signals are routed as differential pairs (LVDS) and are AC-coupled.

Table 35 - Connection between GTP Clock Buffers and FPGA A/B

Signal Name	Clock Buffer	FPGA A/B
CLK_GTX_AB_0p	U59-16	U22-P6
CLK_GTX_AB_0n	U59-15	U22-P5
CLK_GTX_AB_1p	U59-14	U24-AD6
CLK_GTX_AB_1n	U59-13	U24-AD5

The oscillator power supply (U60) is filtered to reduce power supply noise and jitter. Please see the Si534 datasheet for more information.

4.5.5 SATA II Clock Oscillators Circuit

A 150MHz fixed frequency oscillator (X10, X12), P/N LV7745DW-150.0M, is populated to provide a clock source for the SATA II GTP Transceivers, see Figure 31.

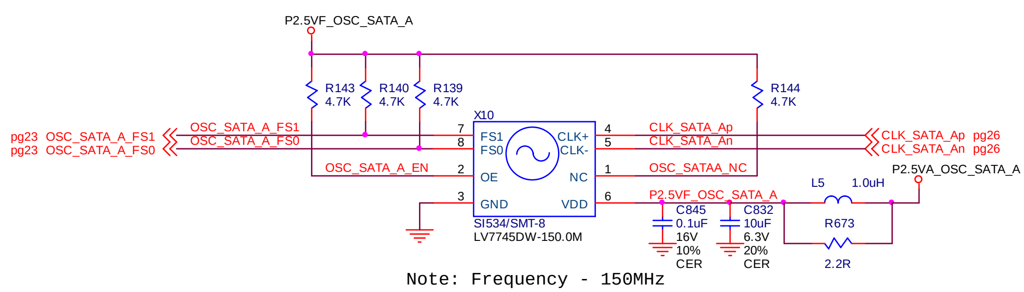


Figure 31 – SATA II Clock Oscillator

4.5.6 Connection between SATA II Clock Oscillators and the FPGAs

The connections between the SATA Clock Oscillators and FPGA A/B are shown in Table 36. These signals are routed as differential pairs (LVDS) and are AC-coupled.

Table 36 - Connection between SATA II Clock Oscillators and FPGA A/B

Signal Name	SATA II Clock Oscillators	FPGA A/B
CLK_SATA_AP	X10-4	U22-AK6
CLK_SATA_AN	X10-5	U22-AK5
CLK_SATA_BP	X12-4	U24-H6
CLK_SATA_BN	X12-5	U24-H5

The oscillator power supply (U57, U62) is filtered to reduce power supply noise and jitter. Please see the LV7745DW-150.0M datasheet for more information.

4.6 Daughter Card (DC) Header Clocks

A single daughter card header is provided on the DN-DualV6-PCIe-4 Logic Emulation Board. The 400 pin MEG-Array connector (P2) on the bottom of the PCBA is used to interface to Dini Group products, e.g. DNMEG_AD-DA. The daughter card header provides a dedicated global LVDS input clock (from daughter card) connected capable pins on FPGA B and a dedicated global LVDS output clock (input to daughter card). In addition, each IO bank provides a source synchronous LVDS clock that connects to FPGA B.

4.6.1 Daughter Card Global Clock Input/Output

DCA_CLK_DN_IN_P/N is a global LVDS input clock to FPGA B (IO Bank 24) and DCA_CLK_UP_OUT_P/N is a global LVDS output clock from the FPGA (IO Bank 24), see Figure 32. Note: These signals are routed as differential pairs (LVDS) and are NOT AC-coupled. Refer to the *Xilinx Virtex-6 Data Sheet* for IO levels and provide DC isolation on the daughter card if required.

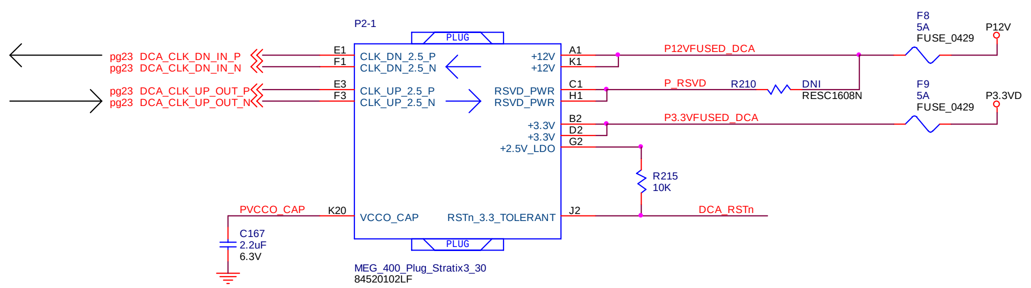


Figure 32 – Daughter Card Global Clock Input/Output

FPGA B has a signal "DCA_CLK_FB_P/N" that is looped back from an output of the FPGA to a clock input on the same FPGA (IO Bank 24), see Figure 33.

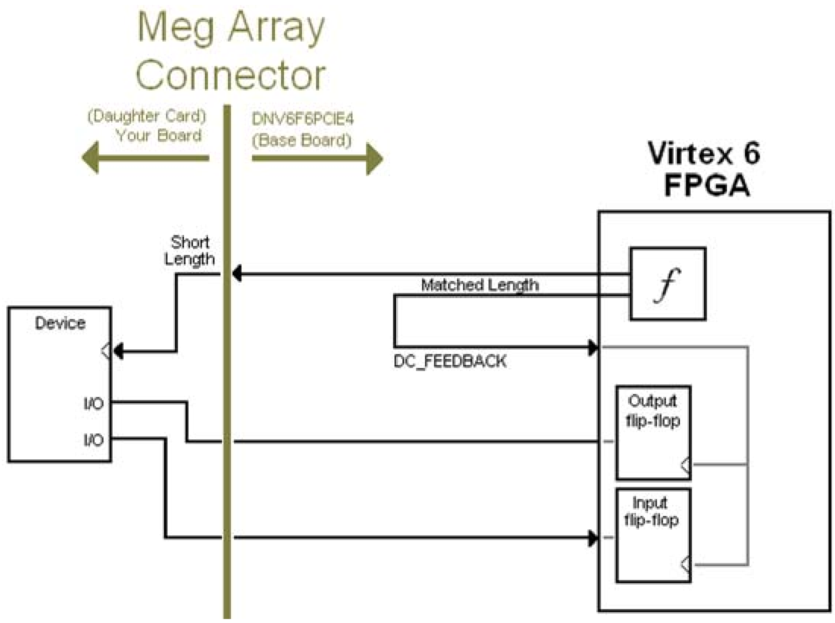


Figure 33 - Daughter Card Header Feedback Clock

The routing length of this feedback clock is equal to the routing length of the signals to the Daughter Card header. This allows the option to have a clock inside the FPGA that is phase aligned with the arrival of the clock at the Daughter Card header

4.6.2 Connection between Daughter Card Header Global Clocks and FPGA B

The connection between the daughter card header global clocks and FPGA B are shown in Table 37.

Table 37 - Connections between Daughter Card and FPGA B

Signal Name	Daughter Card Header	FPGA
DCA_CLK_DN_IN_P	P2-E1	U24-J25
DCA_CLK_DN_IN_N	P2-F1	U24-J24
DCA_CLK_UP_OUT_P	P2-E3	U24-F24
DCA_CLK_UP_OUT_N	P2-F3	U24-F23

4.6.3 Source Synchronous Daughter Card (DC) Header Clocks

Each Daughter Card IO Bank contains a number of clock capable LVDS pairs. _CC nets connect to SRCC and MRCC pins on the FPGA, while _GCC pins connect to global clock inputs on the FPGA and is capable of clocking all signals on the daughter card using synchronous (zero hold time) timing. Note on Virtex-6, this means a GCC pin, a SRCC or MRCC pin on banks 13, 14, 15, 16 and 23, see Figure 34. These clocks

need to comply with the IO requirements of the Virtex-6 FPGA IO bank they are connected too.

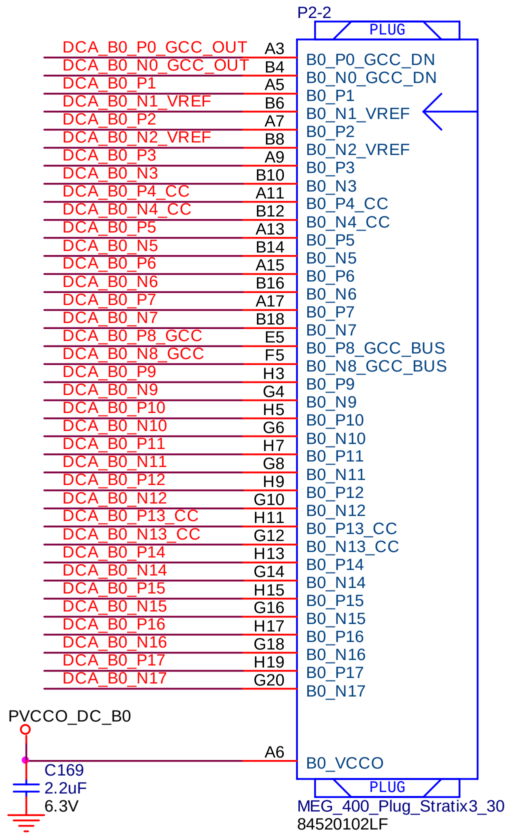


Figure 34 – Secondary Daughter Card (DC) Header Clock

4.6.4 Connection between FPGAs and the Secondary DC Header Clocks

The connection between the Virtex-6 FPGA and the secondary Daughter Card header clocks are shown in Table 38. These signals may be used as inter-connect or clocks.

Table 38 - Connections between FPGA B and y Daughter Card Header Clocks

Signal Name	DC Header	FPGA
DC Bank 0		
DCA_B0_P0_GCC_OUT	P2-A3	U24-AH23
DCA_B0_N0_GCC_OUT	P2-B4	U24-AH24
DCA_B0_P13_CC	P2-H11	U24-AK27
DCA_B0_N13_CC	P2-G12	U24-AJ27
DCA_B0_P4_CC	P2-A11	U24-AH25
DCA_B0_N4_CC	P2-B12	U24-AJ25

Signal Name	DC Header	FPGA
DCA_B0_P8_GCC	P2-E5	U24-AN27
DCA_B0_N8_GCC	P2-F5	U24-AM27
DC Bank 1		
DCA_B1_P13_CC	P2-K11	U24-AD30
DCA_B1_N13_CC	P2-J12	U24-AC30
DCA_B1_P18_CC	P2-C21	U24-AE34
DCA_B1_N18_CC	P2-D22	U24-AF34
DCA_B1_P4_CC	P2-C11	U24-AD29
DCA_B1_N4_CC	P2-D12	U24-AC29
DCA_B1_P8_CC	P2-C19	U24-AE33
DCA_B1_N8_CC	P2-D20	U24-AF33
DC Bank 2		
DCA_B2_P12_CC	P2-H29	U24-N33
DCA_B2_N12_CC	P2-G30	U24-M33
DCA_B2_P18_CC	P2-H21	U24-N28
DCA_B2_N18_CC	P2-G22	U24-N29
DCA_B2_P3_CC	P2-A29	U24-N32
DCA_B2_N3_CC	P2-B30	U24-P32
DCA_B2_P8_CC	P2-A39	U24-L29
DCA_B2_N8_CC	P2-B40	U24-L30
DC Bank 3		
DCA_B3_P12_CC	P2-K29	U24-F31
DCA_B3_N12_CC	P2-J30	U24-E31
DCA_B3_P17_CC	P2-K39	U24-D34
DCA_B3_N17_CC	P2-J40	U24-C34
DCA_B3_P3_CC	P2-C29	U24-K26
DCA_B3_N3_CC	P2-D30	U24-K27
DCA_B3_P8_CC	P2-C39	U24-F33
DCA_B3_N8_CC	P2-D40	U24-G33
DC Bank 3		
DCA_B4_P18_CC	P2-E37	U24-V28
DCA_B4_N18_CC	P2-F37	U24-V27

Signal Name	DC Header	FPGA
DCA_B4_P6_CC	P2-E19	U24-V30
DCA_B4_N6_CC	P2-F19	U24-W30
DCA_B4_P7_CC	P2-E21	U24-V34
DCA_B4_N7_CC	P2-F21	U24-W34
DCA_B4_P8_CC	P2-E23	U24-U31
DCA_B4_N8_CC	P2-F23	U24-U30

4.7 Not Main Bus Clock (NMB)

A dedicated, point-to-point, high-speed (LVDS) "Not Main Bus" (NMB) bus is provided between the Configuration FPGA and FPGA A/FPGA B respectively. A source synchronous clock can be instantiated from any of the signals that connects to a clock capable input.

4.7.1 Not Main Bus (NMB) Clock Circuit

In Source Synchronous mode, QA0[P/N][18-19] can be used as the clock signal. Table 15 shows the connection between the Configuration FPGA and FPGA A, the same applies to FPGA B.

4.8 External Clock Test Point

A three terminal header is provided to allow for an external differential clock (CLK_MUX_TPp/n) input that drives the ICS854057 LVDS Clock Multiplexer. The ICS854057 is a 4:1 LVDS Clock Multiplexer which can operate up to 2GHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The CLKp, CLKn pairs can accept most standard differential input levels. Internal termination is provided on each differential input pair. The ICS854057 operates using a +2.5V supply voltage. The fully differential architecture and low propagation delay make it ideal for use in high speed multiplexing applications. The select pins have internal pull-down resistors.

4.8.1 Multiplexed Global Clock Circuit

Header (J8) allows a LVDS clock input that is multiplexed by the ICS854057 (U6) and drives the G0 clock network, see Figure 27.

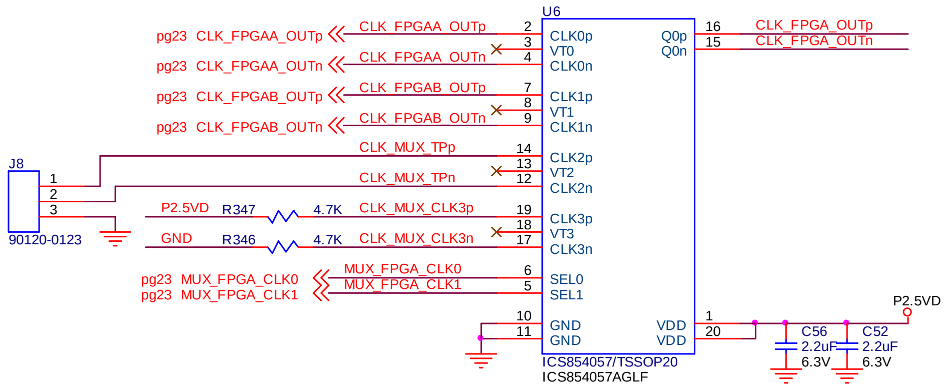


Figure 35 – External Multiplexed Clocks

4.8.2 Connection between External Clock Header and the Clock Multiplexer

The connection between External Clock Header and the Clock Multiplexer are shown in Table 39.

Table 39 - Connection between External Clock Header and Clock Multiplexer

Signal Name	FPGA A/B	Clock MUX 4:1
CLK_FPGAA_OUTp	U22-M23	U6-2
CLK_FPGAA_OUTn	U22-L24	U6-4
CLK_FPGAB_OUTp	U27-F24	U6-7
CLK_FPGAB_OUTn	U27-F23	U6-9
CLK_MUX_TPp	J8-1	U6-14
CLK_MUX_TPn	J8-2	U6-12
MUX_FPGA_CLK0	U17-T10	U6-6
MUX_FPGA_CLK1	U17-T11	U6-5

5 RS232 Port

An RS232 serial port (J1/J6) is provided for low speed communication with the Marvell MV78200 and the Configuration FPGA. The RS-232 standard specifies output voltage levels between –5V to –15V for logical 1 and +5V to +15V for logical 0. Input must be compatible with voltages in the range of -3V to -15V for logical 1 and +3V to +15V for logical 0. This ensures data bits are read correctly even at maximum cable lengths between DTE and DCE, specified as 50 feet.

The RS-232 standard has two primary modes of operation, Data Terminal Equipment (DTE) and Data Communication Equipment (DCE). These can be thought of as host or PC for DTE and as peripheral for DCE. The DN-DualV6-PCIe-4 operates in the DCE mode only.

5.1.1 RS232 Circuit Diagram

Figure 36 shows the implementation of the serial port on the DN-DualV6-PCIe-4 Logic Emulation Board.

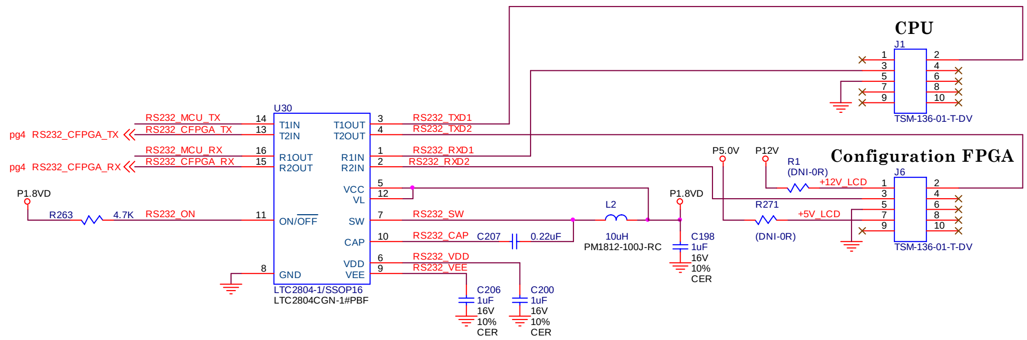


Figure 36 – MCU/Configuration FPGA Serial Port

There are two signals attached to the Configuration FPGA:

- Transmit Data - RS232_CFPGA_TX
- Receive Data - RS232_CFPGA_RX

TX and RX provide bi-directional transmission of transmit and receive data. No hardware handshaking is supported. Note: Signals from the unused LVDS Bus QA[1..4]P/N[0..19] between the Configuration FPGA and FPGA A/B may be used to implement a RS232 port on FPGA A/B.

5.1.2 Connections between RS232 Port and the Configuration FPGA/CPU

The connections between the Configuration FPGA/CPU and the RS232 Port are shown in Table 40.

Table 40 - Connections between RS232 Port and the Configuration FPGA/CPU

Signal Name	RS232 Port	CPU/Header
RS232_MCU_TX	U30-14	U4-AC24
RS232_MCU_RX	U30-16	U4-AD24
RS232_TXD1	U30-3	J1-2
RS232_RXD1	U30-1	J2-3
Signal Name	**RS232 Port**	**Configuration FPGA**
RS232_CFPGA_TX	U30-13	U17-K23
RS232_CFPGA_RX	U30-15	U17-K22
RS232_TXD2	U30-4	J6-2

Signal Name	RS232 Port	CPU/Header
RS232_RXD2	U30-2	J6-3
Signal Name	**Configuration FPGA**	**FPGA A**
QA1P0	U17-W24	U22-AA28
QA1N0	U17-V24	U22-AA29

6 Temperature Sensors

The MAX1617A is a precise digital thermometer that reports the temperature of both a remote sensor and its own package. The remote sensor is a diode-connected transistor—typically a low-cost, easily mounted 2N3904 NPN type—that replaces conventional thermistors or thermocouples. Remote accuracy is ±3°C for multiple transistor manufacturers, with no calibration needed. The remote channel can also measure the die temperature of other ICs, such as microprocessors, that contain an on-chip, diode-connected transistor.

6.1.1 Temperature Sensor Circuit

Each FPGA is connected to a temperature sensor. This sensor measures the temperature of the FPGA silicon die, see Figure 37. The maximum recommended operating temperature of the FPGA is 85 degrees. When the configuration circuitry measures the temperature of any FPGA above 80 degrees, it will immediately un-configure the FPGA, and prevent it from re-configuring.

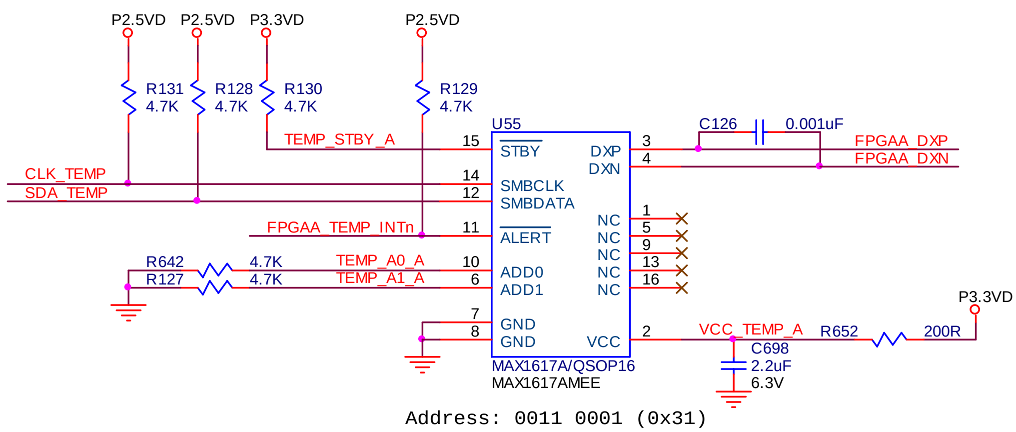


Figure 37 - Temperature Sensor (FPGA A)

When the temperature drops below 80, the configuration circuitry will again allow the FPGA to configure.

The FPGA can safely operate to a maximum of +125°C, but timing is not guaranteed. Use the temperature setting in the ISE place and route tool to make timing allowances

for operating the FPGA out-of-range. The temperature limit can be disabled by a menu option in the configuration interface.

6.1.2 Connection between FPGA A/B and Temperature Sensors

The connection between FPGA A/B and the Temperature Sensors are shown in Table 41.

Table 41 - Connection between FPGA A/B and Temperature Sensors

Signal Name	FPGA	Sensor
CLK_TEMP	U17-G7	U55-14
SDA_TEMP	U17-T9	U55-12
FPGAA_DXP	U22-W18	U55-3
FPGAA_DXN	U22-W17	U55-4
FPGAB_DXP	U24-W18	U64-3
FPGAB_DXN	U24-W17	U64-4

7 LED Indicators

The DN-DualV6-PCIe-4 Logic Emulation board provides various LEDs to indicate that status of the board. The LEDs are turned ON by driving the GATE of the N-MOSFET HIGH, see Figure 38.

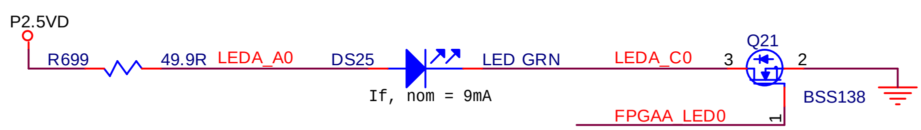


Figure 38 - LED Indicator

7.1 FPGA Status LEDs

Numerous LEDs (Green) are provided to the user as a design aid during debugging. The LEDs can be turned ON by driving the corresponding pin HIGH. Table 42 describes the Status LEDs and their associated pin assignments on the Virtex-6 FPGAs.

Table 42 – FPGA Status LEDs

Signal Name	FPGA	LED
FPGA A (U22)		
FPGAA_LED0	U22-AA23	LED0 (DS25)
FPGAA_LED1	U22-AB23	LED1 (DS24)
FPGAA_LED2	U22-AE23	LED2 (DS23)

Signal Name	FPGA	LED
FPGAA_LED3	U22-AE22	LED3 (DS21)
FPGAA_LED4	U22-AC23	LED4 (DS20)
FPGAA_LED5	U22-AC24	LED5 (DS19)
FPGAA_LED6	U22-AC22	LED6 (DS18)
FPGAA_LED7	U22-AD22	LED7 (DS17)
FPGA B (U24)		
FPGAB_LED0	U24-AA23	LED0 (DS34)
FPGAB_LED1	U24-AB23	LED1 (DS33)
FPGAB_LED2	U24-AE23	LED2 (DS32)
FPGAB_LED3	U24-AE22	LED3 (DS31)
FPGAB_LED4	U24-AC23	LED4 (DS30)
FPGAB_LED5	U24-AC24	LED5 (DS29)
FPGAB_LED6	U24-AC22	LED6 (DS28)
FPGAB_LED7	U24-AD22	LED7 (DS27)
Configuration FPGA (U17)		
CFPGA_LED0	U17-AE13	LED0 (DS12)
CFPGA_LED1	U17-AE12	LED1 (DS13)
CFPGA_LED2	U17-AF23	LED2 (DS14)
CFPGA_LED3	U17-AG23	LED3 (DS15)
CFPGA_LED4	U17-AF13	LED4 (DS16)

7.2 Configuration DONE LEDs

After the FPGAs have received all the configuration data successfully, it releases the DONE pin, which is pulled high by a pull-up resistor. A low-to-high transition on the DONE indicates configuration is complete and initialization of the device can begin. DONE pin drives an N-MOSFET and turns ON a blue LED when the DONE pin goes high. Table 43 describes the DONE LED and its associated pin assignment on the FPGAs.

Table 43 – FPGA DONE LEDS

Signal Name	FPGA	LED
FPGAA_DONE	U26-Y31	DS22
FPGAB_DONE	U22-R8	DS26
CFPGA_DONE	U17-M15	DS10

7.3 Ethernet LEDs

The Gigabit Ethernet Single Port MagJacks (J3) from Tyco contains two LEDs that are controlled by the Ethernet PHY. Table 44 describes the Ethernet LEDs. See the *Marvell 88E1116R Alaska Gigabit Ethernet Transceiver* datasheet for more information on driving the LEDs.

Table 44 – Gigabit Ethernet LEDs

Signal Name	Ethernet PHY	LED
P0_LED0	U1-6	J3-13 (YEL)
P0_LED1	U1-8	J3-15 (ORN)
P0_LED2	U1-9	J3-17 (GRN)

7.4 Power Supply Status LEDs

The LT6700-1 is configured as a simple window comparator to monitor the power supplies. A Power FAULT will be indicated by the RST_PORn signal going active (LOW) and turning on the Reset LED (DS6). The RST_PORn signal can also be activated by enabling the Reset Switch (S1). Table 45 describes the power supply status LEDs and their associated voltage source.

Table 45 – Power Supply Status LEDs

Signal Name	Source Pin	LED
P12V	J5-1, 2, 3	DS44
P1.8VD	PSU4-2, 3	DS41
P2.5VD	PSU5-5	DS37
P3.3VD	PSU2-2, 3	DS38
P5.0V	PSU8-2, 3	Not Monitored
P1.0VD_CPU_CORE	PSU1-2, 3	DS36
P1.1VD_CPU	PSU3-2, 3	DS35
P1.0V_VCCINT_V5	PSU9-5/9	DS43
P1.0V_VCCINT_V6	PSU7-5/9	DS42
P_DIMM_A	PSU11-5/9	DS39
P_DIMM_B	PSU5-5/9	DS40
USB0_OCn	U29-5	DS1

7.5 USB Fault LED

The AP2171 is an integrated high-side power switch optimized for Universal Serial Bus (USB) and other hot-swap applications. The device complies with USB 2.0 and offer current and thermal limiting, including short circuit protection as well as controlled rise time and under-voltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false over-current reporting and will turn on LED (DS1) during an over-current condition, see Table 46.

Table 46 – USB Fault LED

Signal Name	Source Pin	LED
USB0_OCn	U29-5	DS1

7.6 Miscellaneous LEDs

Table 47 describes the miscellaneous status LEDs and their associated source.

Table 47 – Miscellaneous LEDs

Signal Name	Source	LED
Marvell 780200 CPU(U4)		
RST_CPU_MPP13n	U4-AE21	DS3
SATA1_Act#	U4-AF21	DS2
SATA0_Act#	U4-AA22	DS4
Clock Multipliers – LOL Indicators		
SYNTH_LOL_G0	U10-18	DS7
SYNTH_LOL_G1	U16-18	DS9
SYNTH_LOL_G2	U20-18	DS11
Front Panel LED		
LED_BICLR_RED	U17-5	DS45

8 Power Distribution

The DN-DualV6-PCIe-4 Logic Emulation Board supports a wide range of technologies, from legacy devices like serial ports, to DDR3 SDRAM, Ethernet Transceivers and GTP Transceivers on the Xilinx FPGAs. This wide range of technologies, including the various FPGA power supplies requires a variety of power supplies. These are provided on the DN-DualV6-PCIe-4 Logic Emulation Board using a combination of switching and linear power regulators.

8.1 In-System Operation

The primary source of power for the DN-DualV6-PCIe-4 is the PCI Express "graphics" power connector (J5). All other voltages on the board are generated from this supply. During In-System operation, the DN-DualV6-PCIe-4 can be powered from the PCI Express Edge Connector, however the board will exceed the available power from the system (fuse, F12 needs to be installed for this option to be available, see Figure 39).

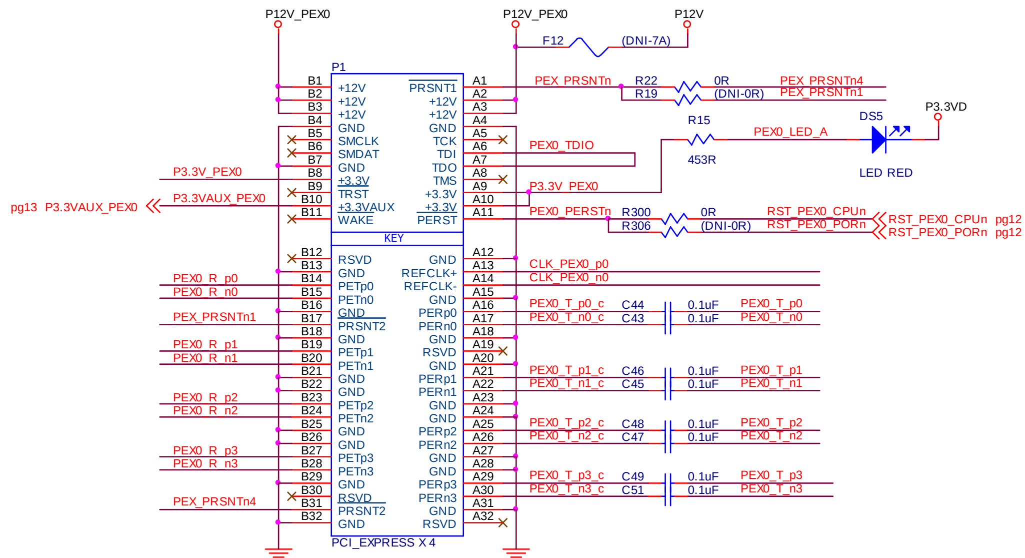
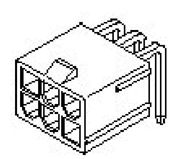


Figure 39 – PCI Express Edge Connector

8.2 Stand Alone Operation

An external ATX power supply is used to supply power to the DN-DualV6-PCIe-4 Logic Emulation Board in stand-alone mode, see Figure 41. The external power supply connects to a "Mini-Fit PCI Express "header J5, Molex P/N 45558-0002.



The user should connect the matching male power connector on the ATX power supply to this header (6-Pin PSU Adaptor for PCIe Video Cards supplied as part of this kit). The DN-DualV6-PCIe-4 Logic Emulation Board has the following shared power supplies; they are generated from the +12V supply on the external power connector (J5).

- PSU8 P5.0V (+5.0V)
- PSU5 P2.5VD (+2.5V)
- PSU4 P1.8VD (+1.8V)
- PSU2 P3.3VD (+3.3V)

Any ATX type power supply is adequate. Dini Group recommends a power supply rated for 450W, see Ultra LSP450, P/N ULT-LSP450. Note that only a 6-pin "PCI Express graphics" cable should be used. This connector easily confused with the now defunct "AUX POWER" connector (also 6-pin) and the 4-and 6-pin EPS "motherboard" connections. The connector is keyed, so the wrong connectors will have difficulty fitting properly into the board.



Figure 40 - ATX Power Supply

8.2.1 External Power Connector

Figure 41 indicates the connections to the external power connector. This header is fully polarized to prevent reverse connection and is rated for 600VAC at 6A per contact. An overvoltage crowbar circuit, utilizing a Diode (D1), is provided to protect the +12V supply.

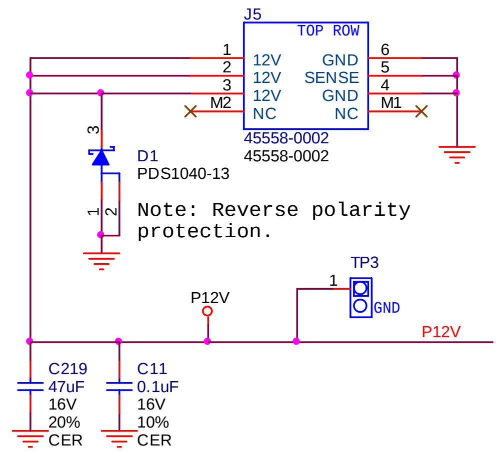


Figure 41 - External Power Connection

Note: Header J5 is not hot-plug able. Do not attach power while power supply is ON.

8.3 Voltage Monitors and Reset

8.3.1 Voltage Monitor

The LT6700-1 is configured as a simple window comparator to monitor the power supplies. A power fault will be indicated by the PWR_FAULTn signal going active (LOW). See 7.4 Power Supply Status LEDs for a description of the power supplies being monitored.

8.3.2 Voltage Monitor Circuit

The comparators have a built-in 400mV reference and each one have one input available externally, see Figure 42. The comparators are configured as a simple window comparator to detect high/low voltage thresholds.

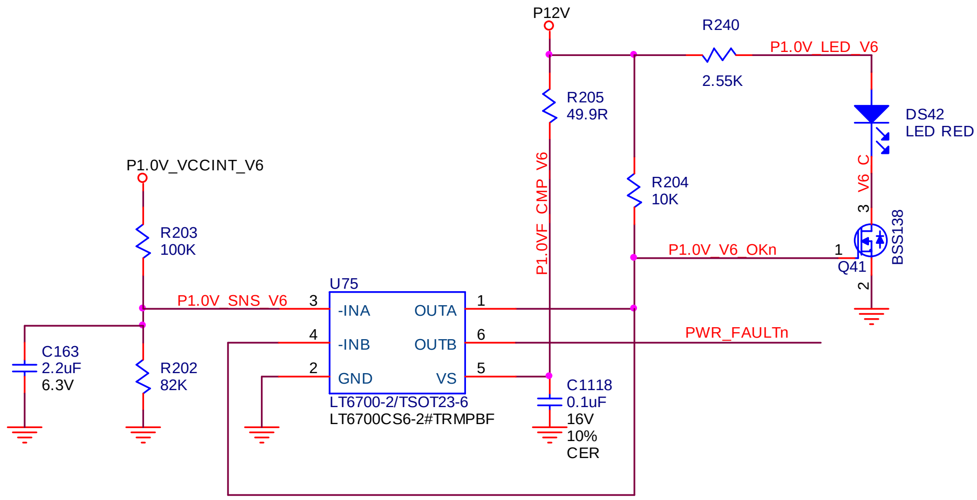


Figure 42 - Low Voltage Comparator Circuit

8.3.3 Power Sequencing

Both the Marvell MV78200 CPU and the Virtex-6 FPGAs have power-up requirements. Please refer to the datasheet for the requirements.

8.3.4 Reset Options

Refer to Figure 43 for a block diagram of the reset topology. FPGA A/B can be reset by the Configuration FPGA, as well as the Power-On-Reset (POR) circuitry.

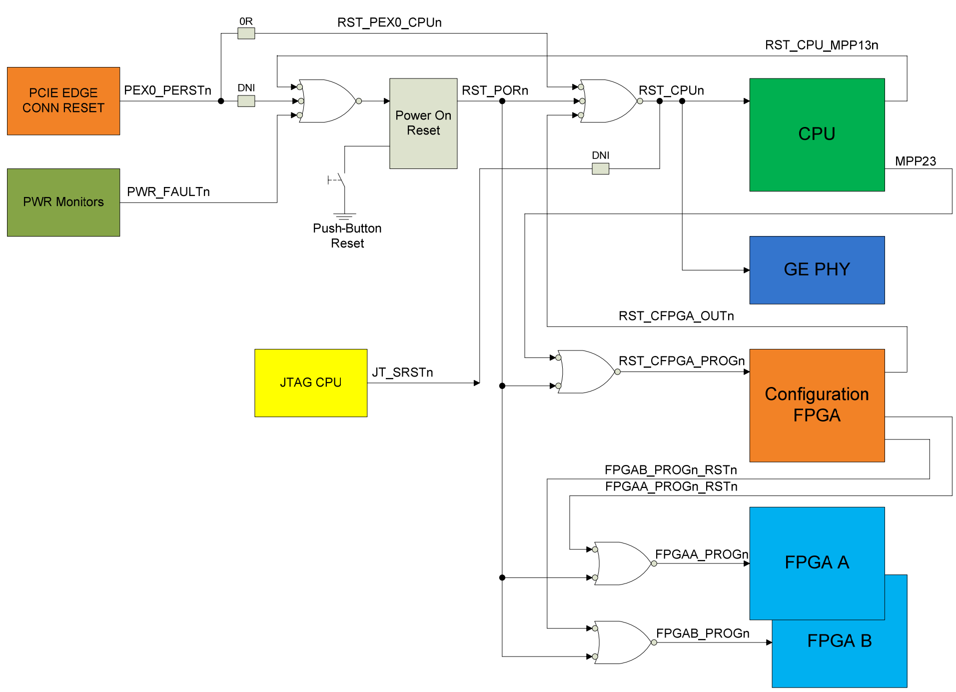


Figure 43 - Reset Block Diagram

Reset inputs from various sources drive the TPS3808 (U7). The TPS3808 microprocessor supervisory circuit monitors system voltages, asserting an open-drain RST_PORn signal when the SENSE voltage drops below a preset threshold or when the manual reset (MRn) pin drops to a logic LOW. The reset delay time can be set by connecting the CT pin to an external capacitor, see Figure 44.

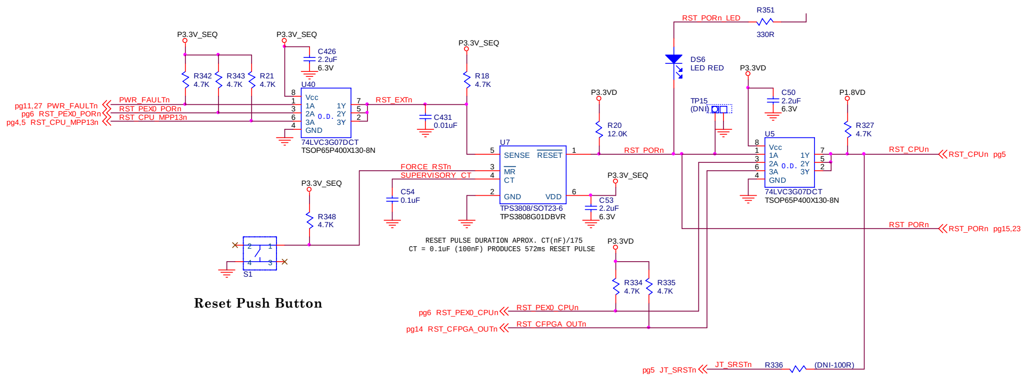


Figure 44 - Reset Circuit

The reset pulse duration is set to approximately 102mS with CT = 0.018uF.

9 Daughter Card Header

One 400-pin MEG-Array daughter card header (P2) is placed on the bottom of the PCB. All signals on the header are routed as matched length, differential, 50-Ohm transmission lines. Other connections on the daughter card connector system include two dedicated, differential clock connections for global clocks, power connections, bank V_{CCO} power, and a reset signal.

9.1 Daughter Card clocking

Refer to Daughter Card (DC) Header Clocks, par 4.6 in this User Manual.

9.2 Daughter Card Header Pin Assignments

The pin assignments of the daughter card header are designed to reduce cross talk to manageable levels while operating at full speed of the Virtex-6 LVDS standards. . The daughter card header is divided into five banks, refer to Figure 45. The Virtex-6 devices support source-synchronous interfacing with LVDS signaling at up to 1.6Gbps. The ground-to-signal ratio of the connector is 1:1, refer to Figure 45. General purpose IO is arranged in a GSGS pattern to allow high speed single-ended or differential use. These signals are routed as loosely-coupled differential signals, meaning when used differentially, they benefit from the noise-resistant properties of a differential pair, but when used in a single-ended configuration, they do not interfere with each other excessively.

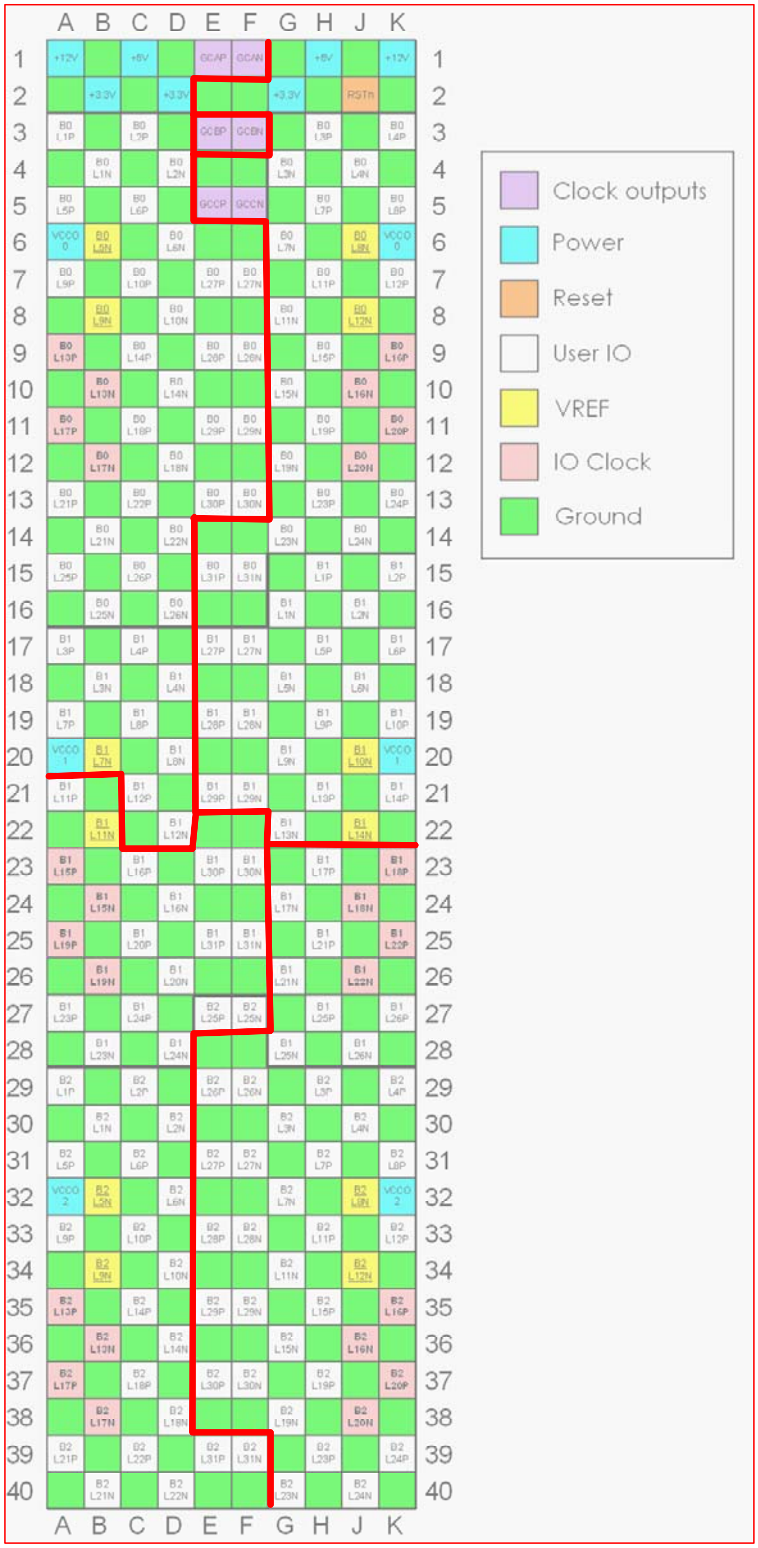


Figure 45 - Daughter Card Header Bank/Pin Assignments

9.3 Special Pins on the Daughter Card Header

9.3.1 CLK_DN_2.5p/n, and CLK_UP_2.5p/n

The daughter card pin-out defines two bidirectional differential clock pins. These clock signals are intended to be used as differential clock signals. These signals are routed to clock capable (MRCC) inputs on the Virtex-6 FPGA and can be used for global clocking.

9.3.2 V_{CCIO} Power Supply

On the Virtex-6 FPGA each IO bank has its own V_{CCO} pins. V_{CCO} is determined by the IO standard for that particular IO bank. Since a daughter card will not always be present on a daughter card connector, a V_{CCO} bias generator is used on the motherboard for each daughter card bank to keep the V_{CCO} pin on the FPGA within its recommended operating range. The Daughter Card drives V_{CCO} to the required level for the particular IO standard. The V_{CCO} impressed by the Daughter Card needs to satisfy the $V_{IH(MAX)}$ of the FPGA on the host board. There are five Adjustable Linear Power Supplies (U25, U26, U28, U66, and U27) on the board, one per daughter card header IO bank, refer to Figure 46. Refer to the datasheet for the LT1963A from Linear Technology on how to adjust the output voltages. R782 allows the user to remove the powers supply if a V_{CCO} of +2.5V is required, since that voltage can be supplied by the system.

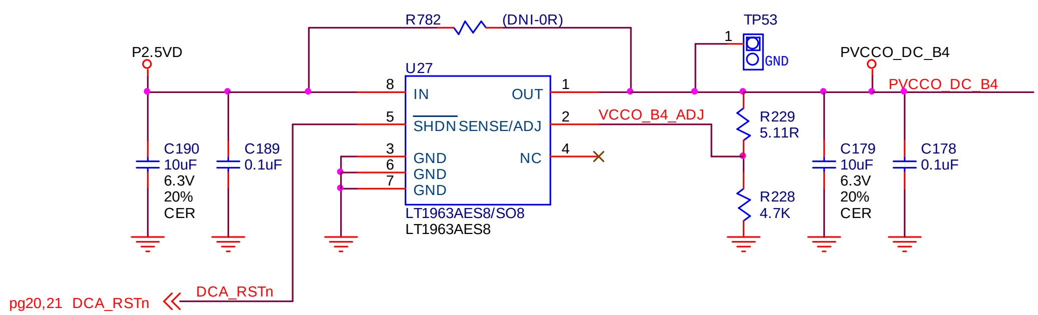


Figure 46 - V_{CCO} Adjustable Linear Power Supply (x5)

9.4 Power and Reset

The +12V and +3.3V power rails can be supplied by the Daughter Card Headers if the fuses are installed, refer to Figure 47. Each pin on the MEG-Array connector is rated to tolerate 1A of current without thermal overload.

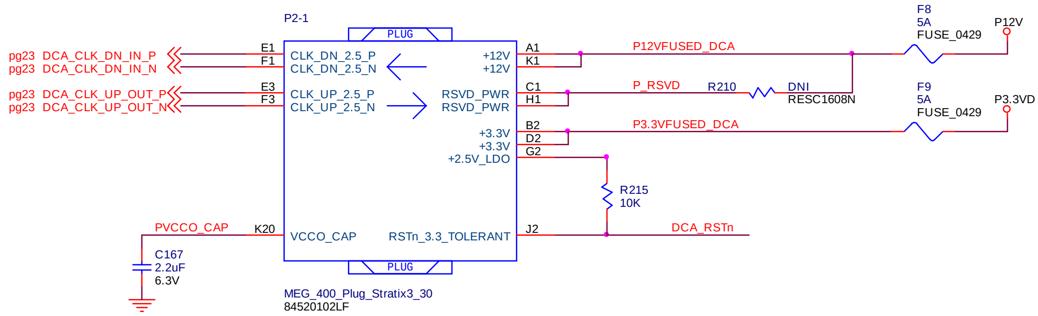


Figure 47 - Daughter Card Header Power & RESET

The "DCA_RSTn" signal is routed from the under voltage reset monitor (U77). The signal is used to hold the V_{CCO} power supplies inactive until the +2.5V supply is stable, in order to meet the Virtex-6 power sequencing requirements, see Table 48.

Table 48 – Daughter VCCO Reset Signal

Signal Name	OD Buffer	Daughter Card Header
DCA_RSTn	U77-6	U25-5, U26-5, U27-5, U28-5, and U66-5

9.5 FPGA to Daughter Card Header IO Connections

Table 49 lists the input/output interconnect between the Virtex-6 FPGA and the Daughter Card header.

Table 49 - FPGA to Daughter Card Header IO Connections

SIGNAL	Daughter Card Receptacle - Bottom	FPGA
DCA_B0_N0_GCC_OUT	P2-B4	U24-AH24
DCA_B0_N1_VREF	P2-B6	U24-AK24
DCA_B0_N10	P2-G6	U24-AN24
DCA_B0_N11	P2-G8	U24-AP29
DCA_B0_N12	P2-G10	U24-AP26
DCA_B0_N13_CC	P2-G12	U24-AJ27
DCA_B0_N14	P2-G14	U24-AM28
DCA_B0_N15	P2-G16	U24-AK28
DCA_B0_N16	P2-G18	U24-AM30
DCA_B0_N17	P2-G20	U24-AH28
DCA_B0_N2_VREF	P2-B8	U24-AK29

SIGNAL	Daughter Card Receptacle - Bottom	FPGA
DCA_B0_N3	P2-B10	U24-AL24
DCA_B0_N4_CC	P2-B12	U24-AJ25
DCA_B0_N5	P2-B14	U24-AL25
DCA_B0_N6	P2-B16	U24-AG26
DCA_B0_N7	P2-B18	U24-AM26
DCA_B0_N8_GCC	P2-F5	U24-AM27
DCA_B0_N9	P2-G4	U24-AP31
DCA_B0_P0_GCC_OUT	P2-A3	U24-AH23
DCA_B0_P1	P2-A5	U24-AJ24
DCA_B0_P10	P2-H5	U24-AN25
DCA_B0_P11	P2-H7	U24-AN29
DCA_B0_P12	P2-H9	U24-AP27
DCA_B0_P13_CC	P2-H11	U24-AK27
DCA_B0_P14	P2-H13	U24-AN28
DCA_B0_P15	P2-H15	U24-AL28
DCA_B0_P16	P2-H17	U24-AN30
DCA_B0_P17	P2-H19	U24-AH27
DCA_B0_P2	P2-A7	U24-AL29
DCA_B0_P3	P2-A9	U24-AK23
DCA_B0_P4_CC	P2-A11	U24-AH25
DCA_B0_P5	P2-A13	U24-AM25
DCA_B0_P6	P2-A15	U24-AG25
DCA_B0_P7	P2-A17	U24-AL26
DCA_B0_P8_GCC	P2-E5	U24-AN27
DCA_B0_P9	P2-H3	U24-AP30
DCA_B1_N0	P2-D4	U24-AC27
DCA_B1_N1	P2-D6	U24-AG32
DCA_B1_N10_VREF	P2-J6	U24-AE32
DCA_B1_N11_VREF	P2-J8	U24-AB33
DCA_B1_N12	P2-J10	U24-AB31
DCA_B1_N13_CC	P2-J12	U24-AC30

SIGNAL	Daughter Card Receptacle - Bottom	FPGA
DCA_B1_N14	P2-J14	U24-AC34
DCA_B1_N15	P2-J16	U24-AA31
DCA_B1_N16	P2-J18	U24-Y26
DCA_B1_N17_VREF	P2-J20	U24-AA33
DCA_B1_N18_CC	P2-D22	U24-AF34
DCA_B1_N2	P2-D8	U24-AD31
DCA_B1_N3	P2-D10	U24-AA29
DCA_B1_N4_CC	P2-D12	U24-AC29
DCA_B1_N5	P2-D14	U24-AC28
DCA_B1_N6	P2-D16	U24-AB26
DCA_B1_N7	P2-D18	U24-AC25
DCA_B1_N8_CC	P2-D20	U24-AF33
DCA_B1_N9	P2-J4	U24-AF31
DCA_B1_P0	P2-C3	U24-AB27
DCA_B1_P1	P2-C5	U24-AG33
DCA_B1_P10	P2-K5	U24-AD32
DCA_B1_P11	P2-K7	U24-AC33
DCA_B1_P12	P2-K9	U24-AB30
DCA_B1_P13_CC	P2-K11	U24-AD30
DCA_B1_P14	P2-K13	U24-AD34
DCA_B1_P15	P2-K15	U24-AA30
DCA_B1_P16	P2-K17	U24-AA25
DCA_B1_P17	P2-K19	U24-AA34
DCA_B1_P18_CC	P2-C21	U24-AE34
DCA_B1_P2	P2-C7	U24-AE31
DCA_B1_P3	P2-C9	U24-AA28
DCA_B1_P4_CC	P2-C11	U24-AD29
DCA_B1_P5	P2-C13	U24-AB28
DCA_B1_P6	P2-C15	U24-AA26
DCA_B1_P7	P2-C17	U24-AB25
DCA_B1_P8_CC	P2-C19	U24-AE33

SIGNAL	Daughter Card Receptacle - Bottom	FPGA
DCA_B1_P9	P2-K3	U24-AG31
DCA_B2_N0	P2-B24	U24-P26
DCA_B2_N1	P2-B26	U24-R27
DCA_B2_N10	P2-G26	U24-M25
DCA_B2_N11	P2-G28	U24-P34
DCA_B2_N12_CC	P2-G30	U24-M33
DCA_B2_N13	P2-G32	U24-R29
DCA_B2_N14	P2-G34	U24-P27
DCA_B2_N15	P2-G36	U24-M32
DCA_B2_N16	P2-G38	U24-N30
DCA_B2_N17	P2-G40	U24-K31
DCA_B2_N18_CC	P2-G22	U24-N29
DCA_B2_N2	P2-B28	U24-M27
DCA_B2_N3_CC	P2-B30	U24-P32
DCA_B2_N4_VREF	P2-B32	U24-P30
DCA_B2_N5_VREF	P2-B34	U24-R32
DCA_B2_N6	P2-B36	U24-L31
DCA_B2_N7	P2-B38	U24-M28
DCA_B2_N8_CC	P2-B40	U24-L30
DCA_B2_N9	P2-G24	U24-T26
DCA_B2_P0	P2-A23	U24-P25
DCA_B2_P1	P2-A25	U24-R28
DCA_B2_P10	P2-H25	U24-N25
DCA_B2_P11	P2-H27	U24-N34
DCA_B2_P12_CC	P2-H29	U24-N33
DCA_B2_P13	P2-H31	U24-P29
DCA_B2_P14	P2-H33	U24-N27
DCA_B2_P15	P2-H35	U24-L33
DCA_B2_P16	P2-H37	U24-M30
DCA_B2_P17	P2-H39	U24-K32
DCA_B2_P18_CC	P2-H21	U24-N28

SIGNAL	Daughter Card Receptacle - Bottom	FPGA
DCA_B2_P2	P2-A27	U24-M26
DCA_B2_P3_CC	P2-A29	U24-N32
DCA_B2_P4	P2-A31	U24-P31
DCA_B2_P5	P2-A33	U24-R31
DCA_B2_P6	P2-A35	U24-M31
DCA_B2_P7	P2-A37	U24-L28
DCA_B2_P8_CC	P2-A39	U24-L29
DCA_B2_P9	P2-H23	U24-R26
DCA_B3_N0	P2-D24	U24-G30
DCA_B3_N1	P2-D26	U24-J29
DCA_B3_N10	P2-J26	U24-J27
DCA_B3_N11	P2-J28	U24-J34
DCA_B3_N12_CC	P2-J30	U24-E31
DCA_B3_N13_VREF	P2-J32	U24-B33
DCA_B3_N14_VREF	P2-J34	U24-H33
DCA_B3_N15	P2-J36	U24-D32
DCA_B3_N16	P2-J38	U24-H30
DCA_B3_N17_CC	P2-J40	U24-C34
DCA_B3_N18	P2-J22	U24-L26
DCA_B3_N2	P2-D28	U24-E33
DCA_B3_N3_CC	P2-D30	U24-K27
DCA_B3_N4	P2-D32	U24-J32
DCA_B3_N5	P2-D34	U24-H32
DCA_B3_N6	P2-D36	U24-B34
DCA_B3_N7	P2-D38	U24-B32
DCA_B3_N8_CC	P2-D40	U24-G33
DCA_B3_N9	P2-J24	U24-K29
DCA_B3_P0	P2-C23	U24-F30
DCA_B3_P1	P2-C25	U24-K28
DCA_B3_P10	P2-K25	U24-J26
DCA_B3_P11	P2-K27	U24-K33

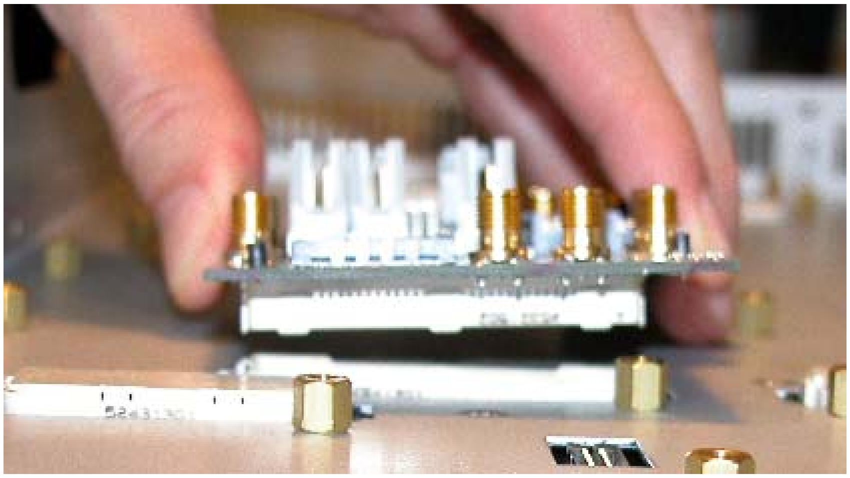
SIGNAL	Daughter Card Receptacle - Bottom	FPGA
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DCA_B3_P13	P2-K31	U24-A33
DCA_B3_P14	P2-K33	U24-H34
DCA_B3_P15	P2-K35	U24-D31
DCA_B3_P16	P2-K37	U24-G31
DCA_B3_P17_CC	P2-K39	U24-D34
DCA_B3_P18	P2-K21	U24-L25
DCA_B3_P2	P2-C27	U24-E32
DCA_B3_P3_CC	P2-C29	U24-K26
DCA_B3_P4	P2-C31	U24-J31
DCA_B3_P5	P2-C33	U24-G32
DCA_B3_P6	P2-C35	U24-C33
DCA_B3_P7	P2-C37	U24-C32
DCA_B3_P8_CC	P2-C39	U24-F33
DCA_B3_P9	P2-K23	U24-J30
DCA_B4_N0	P2-F7	U24-W26
DCA_B4_N1	P2-F9	U24-V25
DCA_B4_N10	P2-F27	U24-T31
DCA_B4_N11_VREF	P2-B20	U24-Y34
DCA_B4_N12	P2-F31	U24-R34
DCA_B4_N13	P2-F25	U24-T29
DCA_B4_N14	P2-F35	U24-T25
DCA_B4_N15	P2-F29	U24-U32
DCA_B4_N16	P2-F39	U24-U27
DCA_B4_N17	P2-F33	U24-V29
DCA_B4_N18_CC	P2-F37	U24-V27
DCA_B4_N2	P2-F11	U24-Y29
DCA_B4_N3	P2-F13	U24-Y31
DCA_B4_N4	P2-F15	U24-W32
DCA_B4_N5	P2-F17	U24-Y27
DCA_B4_N6_CC	P2-F19	U24-W30

SIGNAL	Daughter Card Receptacle - Bottom	FPGA
DCA_B4_N7_CC	P2-F21	U24-W34
DCA_B4_N8_CC	P2-F23	U24-U30
DCA_B4_N9_VREF	P2-B22	U24-T34
DCA_B4_P0	P2-E7	U24-W27
DCA_B4_P1	P2-E9	U24-W25
DCA_B4_P10	P2-E27	U24-T30
DCA_B4_P11	P2-A19	U24-Y33
DCA_B4_P12	P2-E31	U24-R33
DCA_B4_P13	P2-E25	U24-T28
DCA_B4_P14	P2-E35	U24-U25
DCA_B4_P15	P2-E29	U24-U33
DCA_B4_P16	P2-E39	U24-U26
DCA_B4_P17	P2-E33	U24-U28
DCA_B4_P18_CC	P2-E37	U24-V28
DCA_B4_P2	P2-E11	U24-W29
DCA_B4_P3	P2-E13	U24-Y32
DCA_B4_P4	P2-E15	U24-W31
DCA_B4_P5	P2-E17	U24-Y28
DCA_B4_P6_CC	P2-E19	U24-V30
DCA_B4_P7_CC	P2-E21	U24-V34
DCA_B4_P8_CC	P2-E23	U24-U31
DCA_B4_P9	P2-A21	U24-T33
DCA_CLK_DN_IN_N	P2-F1	U24-J24
DCA_CLK_DN_IN_P	P2-E1	U24-J25
DCA_CLK_FB_N	U24-G23	U24-V23
DCA_CLK_FB_P	U24-H23	U24-U23
DCA_CLK_UP_OUT_N	P2-F3	U24-F23
DCA_CLK_UP_OUT_P	P2-E3	U24-F24

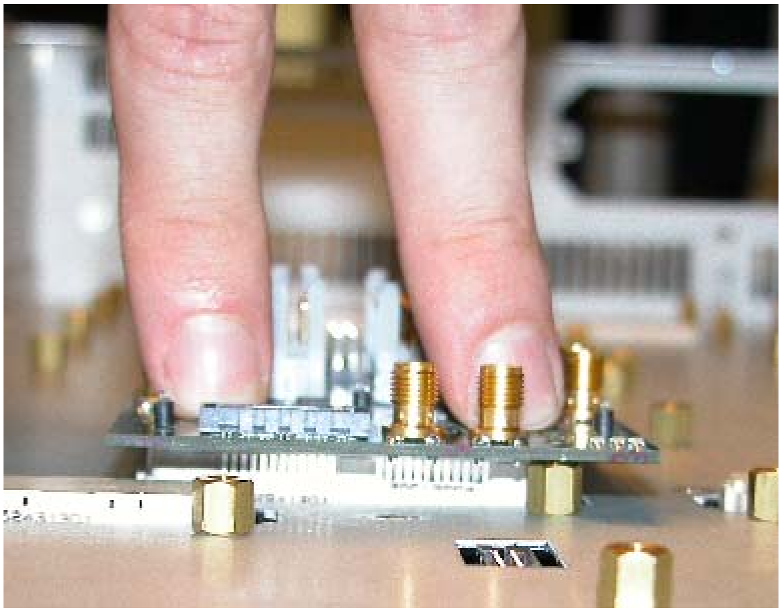
9.6 Insertion/Removal of Daughter Card

Due to the high density MEG-Array connectors, the pins on the plug and receptacle of the MEG-Array connectors are very delicate. When plugging in a daughter card, make

sure to align the daughter card first before pressing on the connector. *Be absolutely certain that both the small and the large keys at the narrow ends of the MEG-Array headers line up BEFORE applying pressure to mate the connectors!*



Place it down flat, then press down gently.



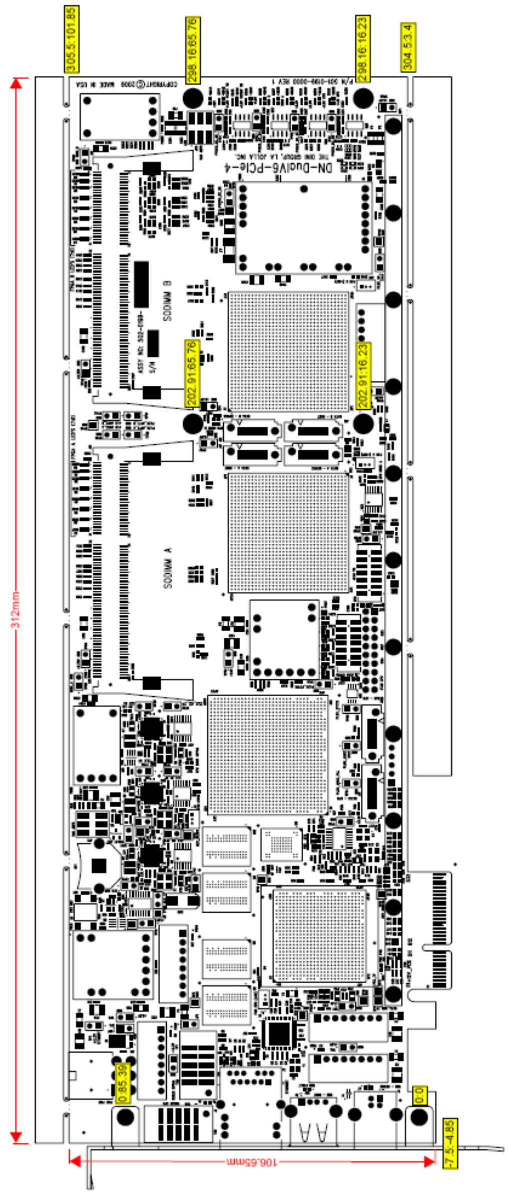
9.7 MEG-Array Specifications

Manufacturer	FCI
Part Number	84520-102LF – Bottom Plug (P4, P5, P6)
RoHS Lead Free Compatible	yes
Total Number Of Positions	400
Contact Area Plating	0.76 µm (30 µin.) gold over 0.76 µm (30 µin.) nickel
Mating Force	30 grams per contact average
Unmating Force	20 grams per contact average
Insulation Resistance	1000 M ohms
Withstanding Voltage	200 VAC
Current Rating	0.45 amps
Contact Resistance	20 to 25 m ohms max (initial), 10 m ohms max increase (after testing)
Temperature Range	-40 °C to +85 °C
Trademark	MEG-Array®
Approvals and Certification	UL and CSA approved
Product Specification	GSe -12-100, from FCI websit
Pick-up Cap	yes
Housing Material	LCP
Contact Material	Copper Alloy
Durability (Mating Cycles)	50

10 Mechanical

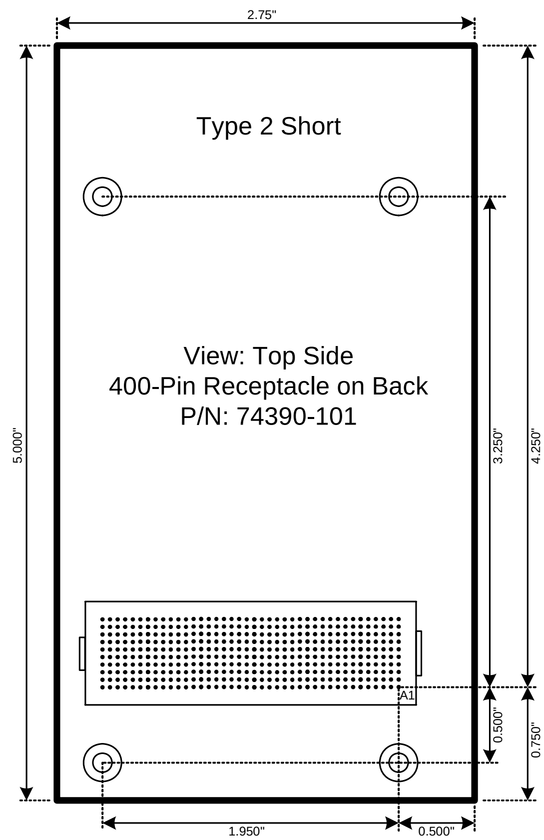
10.1 Board Dimensions

The DN-DualV6-PCIe-4 Logic Emulation Board conforms to the Standard Height PCI Express Add-in Card Form factor. One bus bar (MP1) is installed to prevent flexing of the PWB. The mounting holes are connected to the ground plane and can be used to ground test equipment. The user must not short any power rails or signals to these metal bars - they can conduct a lot of current. Mounting holes are provided to allow the PCB to be mounted in a case.



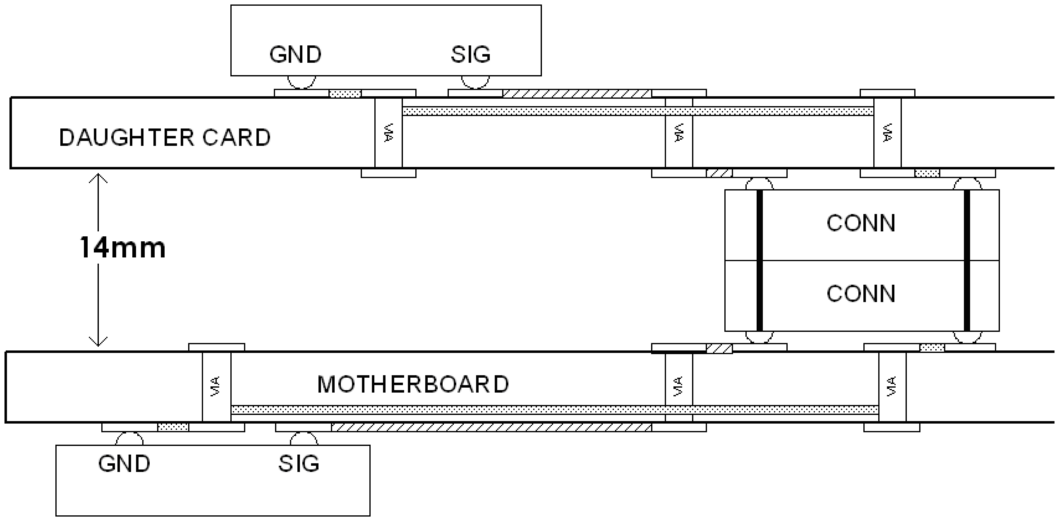
10.2 Standard Daughter Card Size

The DN-DualV6-PCIe-4 Logic Emulation Board provides mounting hole locations for a Daughter Card with the dimensions given below. The DNMEG_Obs Daughter Card product conforms to these dimensions.



10.3 Daughter Card Spacing

With this host-plate-daughter card arrangement, there is a limited Z dimension clearance for backside components on the daughter card. This dimension is determined by the daughter card designer's part selection for the MEG-Array receptacle.



Note that the components on the topside of the daughter card and DN-DualV6-PCIe-4 face in opposite directions.

Chapter 5

Appendix

11 Appendix A: UCF File

See the Customer Support Package (USB Flash Drive) for the Xilinx User Constraint Files (UCF) for FPGA A.

12 Ordering Information

Request quotes by emailing sales@dinigroup.com. For technical questions email support@dinigroup.com